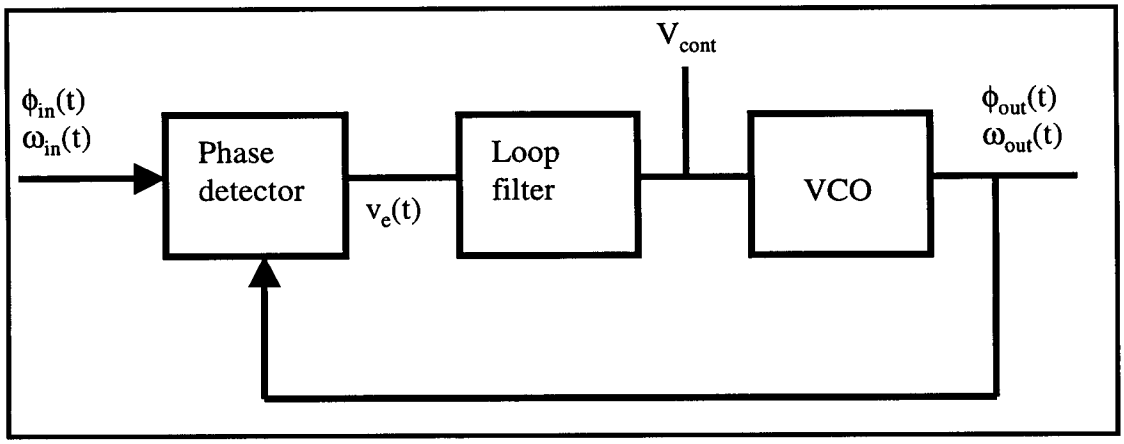
Phase Locked Loop Circuits
ECE145B/ECE218B

Reading: General PLL Description: T. H. Lee, Chap. 15. Gray and Meyer, 10.4.

1. **Definition.** A PLL is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock. This enables the PLL to be used as a control system allowing one system to track with another.

$$\phi_{out}(t) = \phi_{in}(t) + const.$$
$$\omega_{out}(t) = \omega_{in}(t)$$

The PLL output can be taken from either V_{cont}, the filtered (almost DC) VCO control voltage, or from the output of the VCO depending on the application. Either phase or frequency can be used as the input variables.



Of course, phase and frequency are interrelated by:

$$\omega(t) = \frac{d\phi}{dt}$$

$$\phi(t) = \phi(0) + \int_0^t \omega(t')dt'$$

2. Phase detector: compares the phase at each input and generates an error signal, $v_e(t)$, proportional to the phase difference between the two inputs. K_D is the gain of the phase detector (V/rad).

$$v_e(t) = K_D[\phi_{out}(t) - \phi_{in}(t)]$$

As one familiar circuit example, an analog multiplier or mixer can be used as a phase detector. Recall that the mixer takes the product of two inputs. $v_e(t) = A(t)B(t)$. If,

$$A(t) = A\cos(\omega_0 t + \phi_A)$$
$$B(t) = B\cos(\omega_0 t + \phi_B)$$

$$\text{Then,}\quad A(t)B(t) = (AB/2)[\cos(2\omega_0 t + \phi_A + \phi_B) + \cos(\phi_A + \phi_B)]$$

Since the two inputs are at the same frequency when the loop is locked, we have one output at twice the input frequency and an output proportional to the cosine of the phase difference. The doubled frequency component must be removed by the lowpass loop filter. The phase difference then is ideally a DC signal, the control voltage to the VCO.

3. VCO. In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output.

$$\phi_{out} = K_O \int_{-\infty}^{t} V_{cont}\, dt'$$

The VCO oscillates at an angular frequency, ω_{out}. Its frequency is set to a nominal ω_0 when the control voltage is zero. Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient K_0 (rad/s/v).

$$\omega_{out} = \omega_0 + K_O V_{cont}$$

PLL response: To see how the PLL works, suppose that we introduce a frequency step at the input

$$\omega_{in} = \omega_o + \Delta\omega$$

This will cause the phase difference to grow with time since a frequency step is a phase ramp. This in turn causes the control voltage, Vcont, to increase, moving the VCO frequency up to catch up with the input reference signal.

Overshoot in phase will occur if $\omega_{osc} = \omega_{in}$ before $\phi_{osc} - \phi_{in}$ = constant. The frequency will continue to increase until the phase of the v catches up to the input.

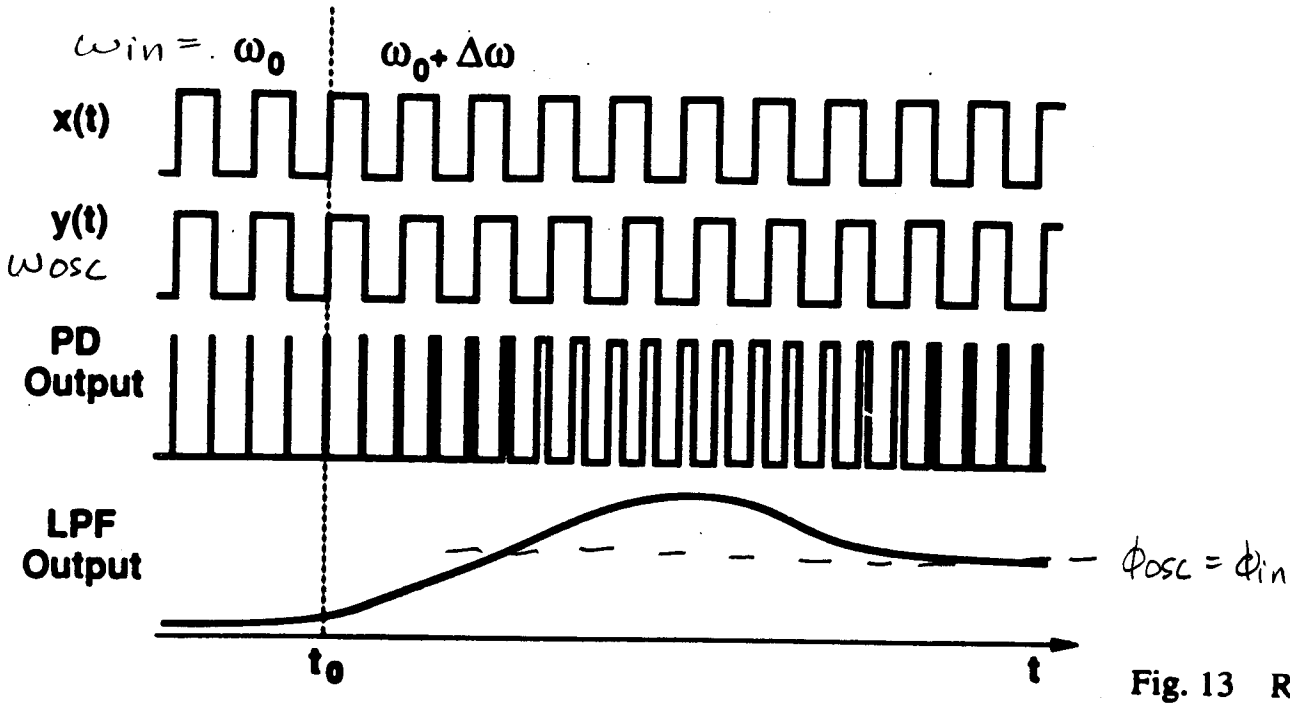
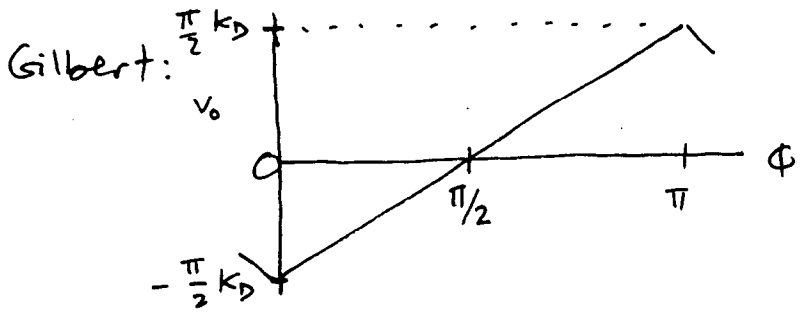


Fig. 13 R

LPF integrates PD output

4. Lock Range. Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the phase detector or the VCO frequency range.

a. If limited by phase detector:



$0 < \phi < \pi$ is the active range where lock can be maintained.

$$V_{o\text{-}max} = \pm K_D \, \pi/2$$

When the phase detector output voltage is applied through the loop filter to the VCO,

$$\Delta\omega_{out-max} = \pm K_v \, \pi/2 \; = \; \omega_L \text{ (lock range)}$$

This is the frequency range around the free running frequency that the loop can track.

Doesn't depend on the loop filter

Does depend on DC loop gain

b. The lock range could also be limited by the tuning range of the VCO. Oscillator tuning range is limited by capacitance ratios or current ratios and is also limited. In many cases, the VCO can set the maximum lock range.

5. Capture range: Range of input frequencies around the VCO center frequency onto which the loop will lock when starting from an unlocked condition. Sometimes a frequency detector is added to the phase detector to assist in initial acquisition of lock.

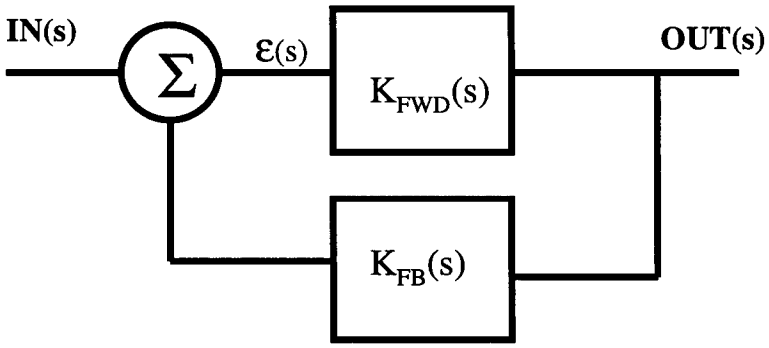
6. Approach: We will discuss the details of phase detectors and loop filters as we proceed. But, at this point, we will treat the PLL as a linear feedback system. We assume that it is already "locked" to the reference signal, and examine how the output varies with the loop transfer function and input. A frequency domain approach will be used, specifically describing transfer functions in the s-domain.

$$Ve(s)/\Delta\phi = K_D$$

$$\phi_{out}(s)/V_{cont}(s) = K_O/s$$

Note that the VCO performs an integration of the control voltage and thus provides a factor of 1/s in the loop transfer function. Because of this, a PLL is always at least a first order feedback system.

PLL is a feedback system



Loop Gain: $T(s) = K_{FWD}(s)\,K_{FB}(s)$

Transfer Function: $\dfrac{OUT(s)}{IN(s)} = H(s) = \dfrac{K_{FWD}(s)}{1+T(s)}$

The Loop gain can be described as a polynomial:

$$T(s) = \frac{K'(s+a)(s+b)\cdots}{s^n\,(s+\alpha)(s+\beta)\cdots}$$

ORDER = the order of the polynomial in the denominator

TYPE = n (the exponent of the s factor in the denominator)

PHASE ERROR = $\varepsilon(s) = \dfrac{IN(s)}{1+T(s)}$

STEADY STATE ERROR = $\varepsilon_{SS} = \lim_{s\to 0}[s\varepsilon(s)] = \lim_{t\to\infty}\varepsilon(t)$

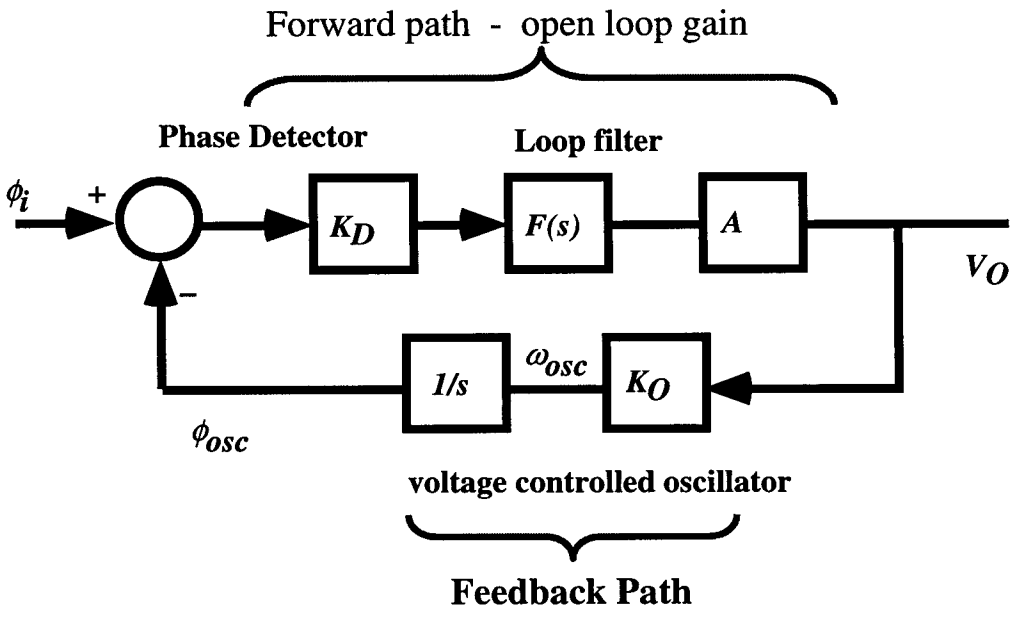
(this is the Laplace Transform final value theorem)

SS error is a characteristic of feedback control systems. This is the error remaining in the loop at the phase detector output after all transients have died out.

7. **Applications:** There are many applications for the PLL, but we will study three:
   a. FM demodulator
   b. Frequency synthesizer
   c. Clock generation

You should note that there will be different input and output variables and different design criteria for each case, but you can still use the same basic loop topology and analysis methods.

A. **FM Demodulator**. (See Gray and Meyer, Chap. 10, Section 4.)



$$\frac{V_O}{\phi_i} = \frac{K_D F(s)\, A}{1 + K_D F(s)\, A(K_O / s)}$$

$$\frac{V_O}{\omega_i} = \frac{1}{s}\frac{V_O}{\phi_i} = \frac{K_D F(s)\, A}{s + K_D F(s)\, A\, K_O}$$

For convenience, we define $K_v = K_D K_O A$

How does the PLL work as an FM demodulator?

Frequency to voltage conversion: We need to convert the frequency variation of the input signal to a baseband signal whose frequency is equal to f_m, the modulation frequency, and whose amplitude is equal to Δf, the frequency deviation. The input carrier frequency will be centered at the IF frequency, but will vary in time around this frequency.

Input Variable: $\omega_i = \omega_c + \Delta\omega \sin \omega_m t$

Output Variable: $V_O = {}^{\Delta\omega}/_{K_O} \sin \omega_m t$

In the FMD application, the output is the VCO control voltage, not the phase of the VCO. This voltage will track the input FM signal modulation frequency and deviation. The loop filter is lowpass. The block A represents a gain factor, usually 1 with a passive LPF, but it can be higher if the filter is implemented with an active filter.

Assume that the loop is locked at the IF frequency, ω_c. Frequency modulation will shift the instantaneous frequency around ω_c by $\Delta\omega$ at rate ω_m. As the frequency shifts with time, the phase detector will sense a phase error that increases with time. The filtered error voltage, Vcont = V_o, will send the VCO closer to $\omega_c + \Delta\omega$, tracking the frequency shift. If the bandwidth of the loop is greater than ω_m, the loop will track the frequency deviation of the input signal and V_o will be the demodulated baseband signal, $\Delta\omega/K_o \sin(\omega_m t)$.

Now we will consider the frequency and time response of a PLL in the FMD application. The loop filter transfer function F(s) has a big influence on these responses.

Case 1. FIRST ORDER LOOP

Let $F(s) = 1$ (no loop filter)

$$\frac{V_o(s)}{\omega_i} = \frac{1}{K_o}\left(\frac{K_V}{s + K_V}\right)$$

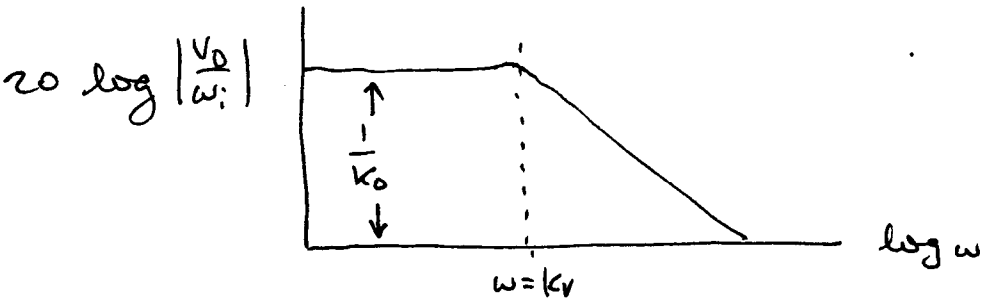
loop bandwidth Low pass transfer function

$$\left|\frac{V_o(j\omega)}{\omega_i}\right| = \frac{1}{K_o}\,\frac{K_V}{\sqrt{\omega^2 + K_V^2}} = \frac{1}{\sqrt{2}}$$

$$\omega_{3dB} = K_V$$

time const. Single pole network response

$$\tau = \frac{1}{K_V}$$



lock range.

$$\omega_{LOCK} = \pm K_V \frac{\pi}{2}$$

(or limit of VCO tuning)

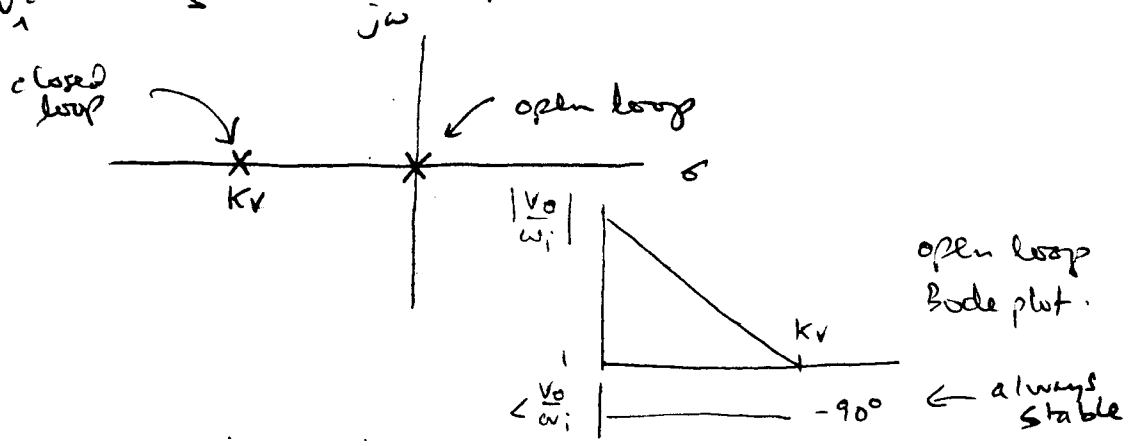
What if loop is open?

$$\frac{V_o}{\phi_i} = \frac{K_D A}{1 + K_D A \cdot 0} = K_D A$$

no FB

$$\frac{V_o}{\omega_i} = \frac{K_D A}{s}$$

pole at $s = 0$

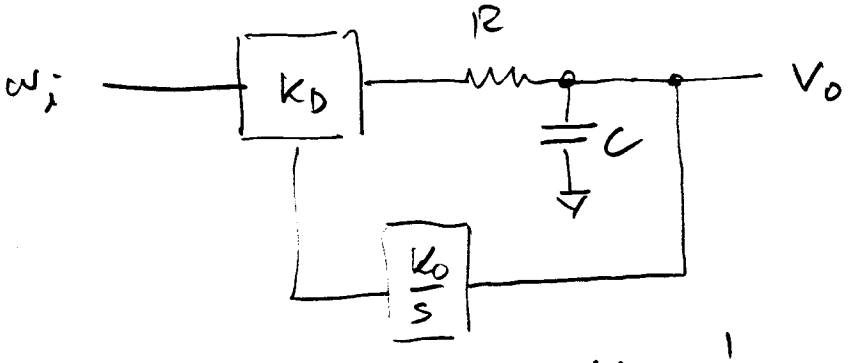


So, what are the problems with first order loop?

1. Doesn't filter out $2\omega_o$ component from phase detector.
2. You can't have high K_V (good for tracking) and narrow bandwidth at the same time.

BODE.

$$F(s) = \frac{1}{1 + s/\omega_1}$$

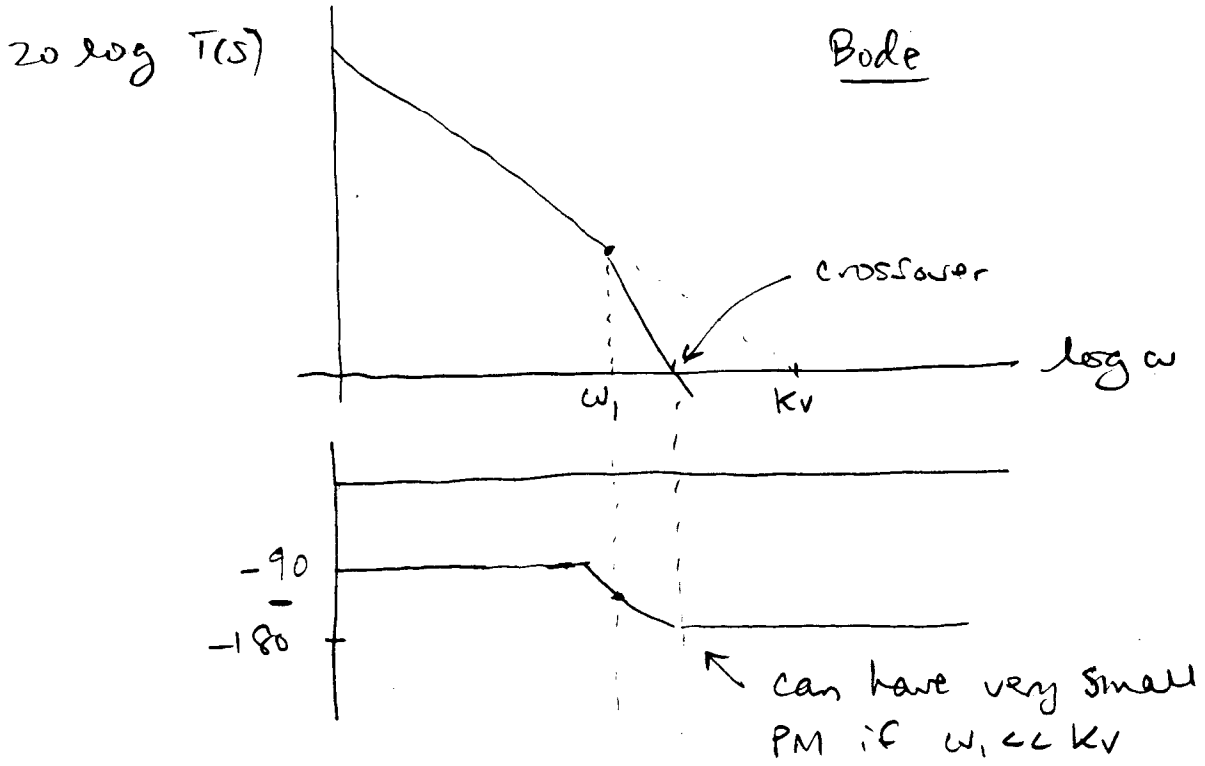


$$\omega_1 = \frac{1}{RC}$$

$$K_v = K_o K_D$$

$$T(s) = \frac{K_D K_o}{s\left(1 + \frac{s}{\omega_1}\right)}$$

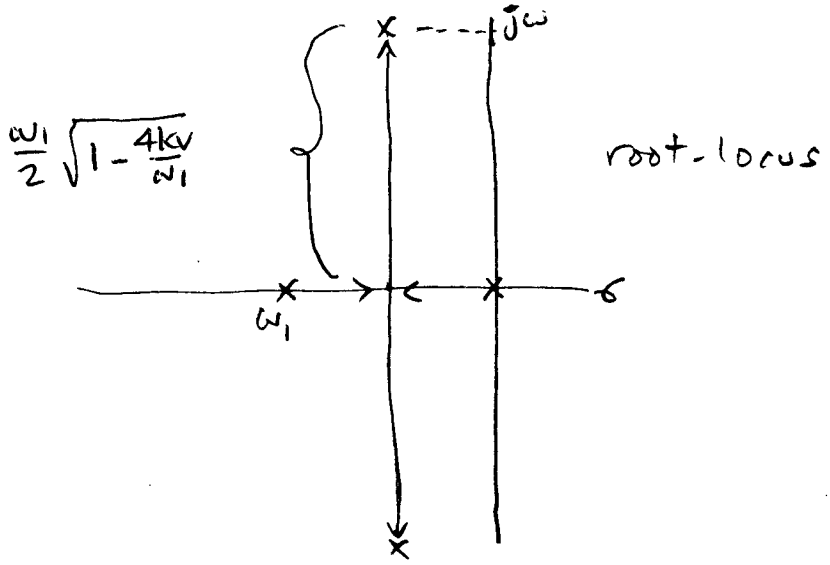
loop gain



Root-Locus

Closed loop response: $\frac{V_o}{\omega_i} = \frac{1}{K_0}\left(\frac{1}{1+\frac{s}{K_v}+\frac{s^2}{\omega_1 K_v}}\right)$

$$s = -\frac{\omega_1}{2}\left(1 \pm \sqrt{1-\frac{4K_v}{\omega_1}}\right)$$



can have very underdamped response when $\omega_1 << k$

so, again, narrow bandwidth and high K_v are not achievable

We could also define ω_n and ζ for this case.

$$\frac{V_o}{\omega_i} = \frac{1}{K_0}\left(\frac{1}{\frac{s^2}{\omega_n^2} + \frac{2\zeta}{\omega_n}s + 1}\right)$$

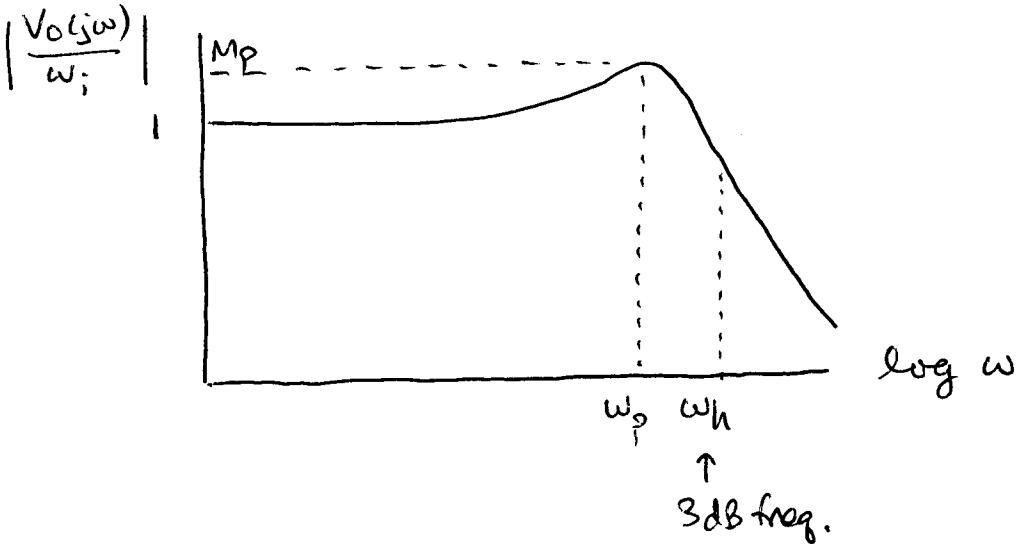
so we can see

$$\omega_n = \sqrt{K_v \omega_1}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_v}}$$

Clearly, if $\omega_1 << K_v$, ζ is small and we have low damping.

Gain response. use formulas for second-order lowpass (Lee Sec. 14.11.2)



We might prefer a flat gain response for our FMD. We are modulating the carrier ω_c with ω_m. The output of the FMD should not have a gain peak. Also, $\omega_h \gg \omega_{m,max}$.

$$M_p = \frac{1}{2\zeta\sqrt{1-\zeta^2}} \qquad \text{for } \zeta < \frac{1}{\sqrt{2}}$$

if we set $\zeta = \frac{1}{\sqrt{2}}$, $M_p = 1$, thus, no gain pe

$$\omega_h = \omega_n\left[1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\,\right]^{1/2}$$

The 3dB BW $\omega_h = \omega_n$ when $\zeta = \frac{1}{\sqrt{2}}$.

So, this gives us:

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_V}} = \frac{1}{\sqrt{2}}$$

or $\boxed{\omega_1 = 2K_V}$

$$\omega_h = \omega_n = \sqrt{K_V \omega_1} = \sqrt{2}\,K_V$$

So what have we accomplished so far?

We have removed the $2\omega_c$ output from the phase detector, but:

1. To avoid underdamping, ω_l and k_v are related. So we can't have a narrow loop bandwidth (noise filtering) and a wide locking range at the same time since

$$\omega_l = \pm k_v \frac{\pi}{2}$$

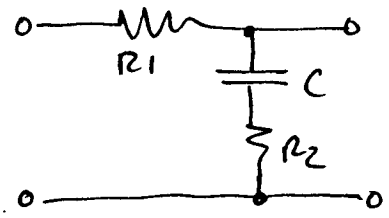
2. The compromise with $\zeta = \frac{1}{\sqrt{2}}$ doesn't provide a flexible solution.

So, ω_1 and K_V are not truly independent. A narrow loop bandwidth can still only be obtained by reducing the lock range.

We can solve this problem by adding a zero to the loop filter.

> Recall from our discussion of feedback amplifiers how a feedback zero changed the root-locus. Here we are putting the zero in the forward path but it has similar benefits.

Add zero to F(s):



$$F(s) = \frac{1 + s/\omega_2}{1 + s/\omega_1}$$

$$\omega_2 = \frac{1}{CR_2}$$

$$\omega_1 = \frac{1}{C(R_1+R_2)} < \omega_2$$

$\omega_2 > \omega_1$

show FIG. 10.23 (G&L)

Substitute F(s) into the FB transfer function

$$\frac{V_O}{\omega_1} = \frac{K_D F(s)}{s + K_D K_O F(s)}$$

$$= \frac{K_D (1 + s/\omega_2)}{\frac{s^2}{\omega_1} + \left(1 + \frac{K_V}{\omega_2}\right) s + K_O K_D}$$

$$= \frac{1}{K_O} \frac{(1 + s/\omega_2)}{\frac{s^2}{K_V \omega_1} + \left(\frac{1}{K_V} + \frac{1}{\omega_2}\right) s + 1}$$

So,

$$\omega_n = \sqrt{K_V \omega_1}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_V}} + \frac{1}{2}\frac{\omega_n}{\omega_2}$$

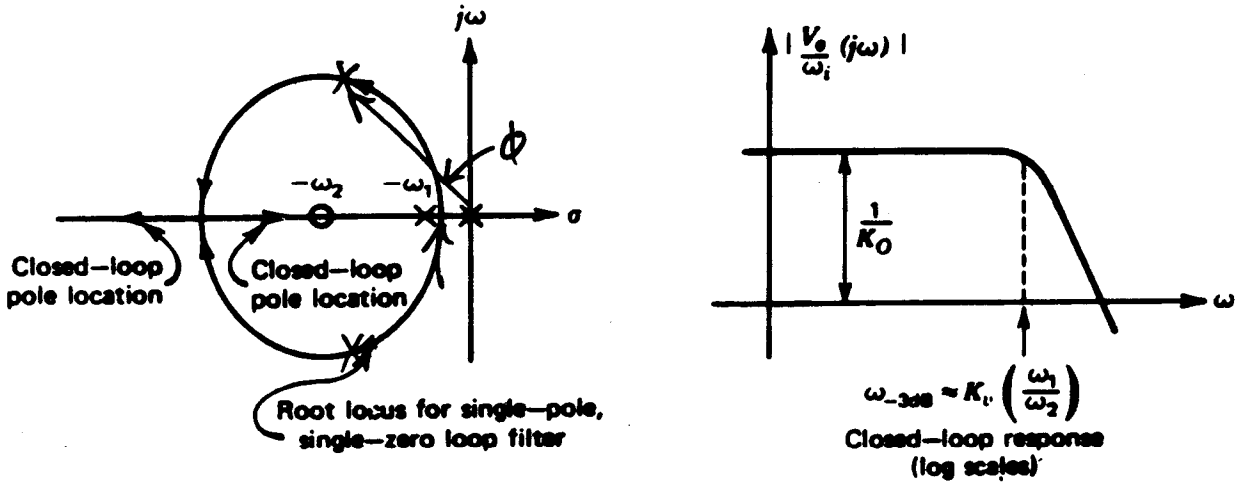
added term due to zero increases damping

if $\zeta = \frac{1}{\sqrt{2}}$,

$$\omega_2 \cong \frac{\omega_n}{\sqrt{2}}$$

set $T(s) = 0$

open loop: $\frac{V_o}{\omega_i} = \frac{K_D(1 + s/\omega_2)}{s(1 + s/\omega_1)}$ poles at $s = 0$, $s = -\omega_1$; zero at $s = -\omega_2$



(d)

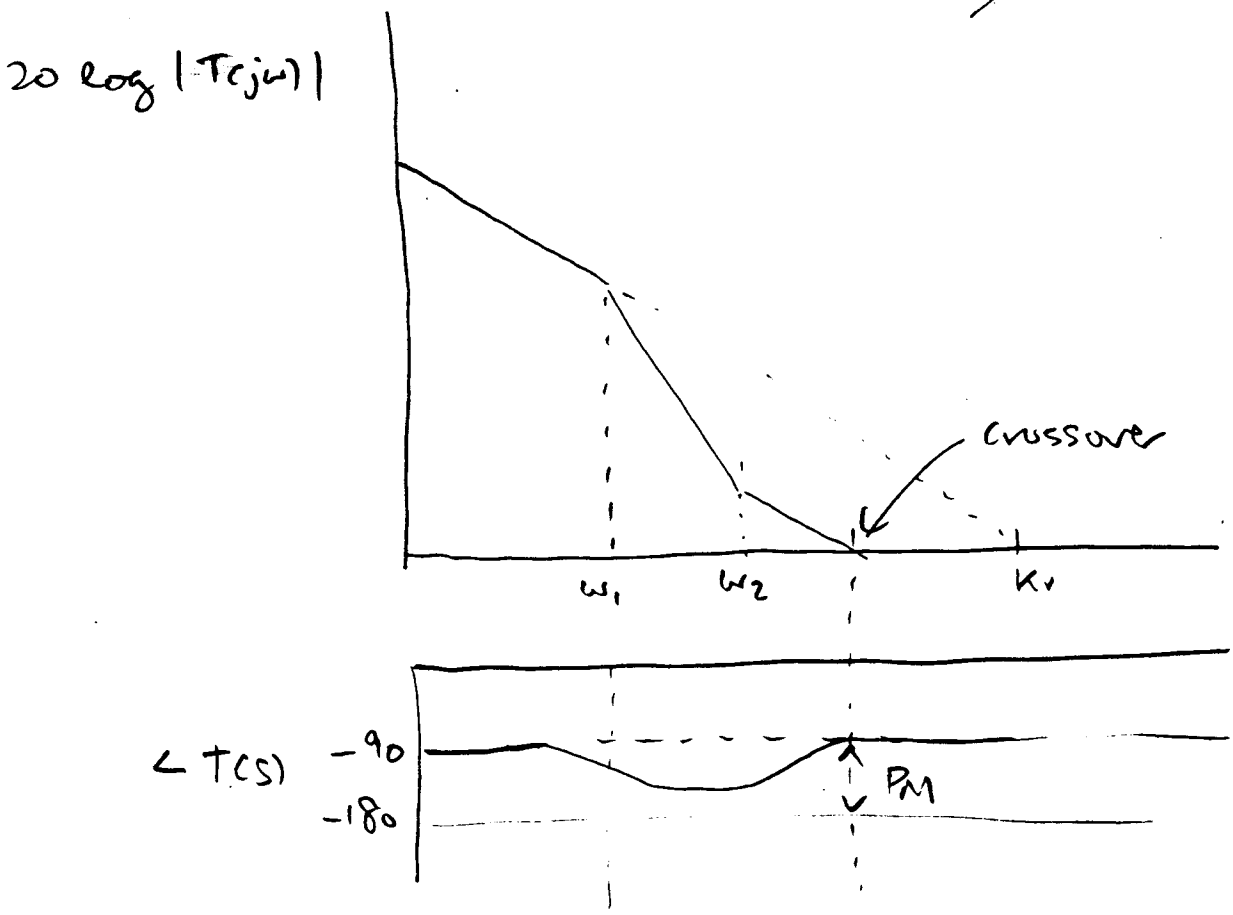
Figure 10.23d Root locus and frequency response of a second-order PLL with a zero. Frequency response shown is for large loop gain such that poles are located as shown in the root locus.

Adding a zero to the transfer function helps the transient response and gain response. But now we cannot use all of the formulas in Lee's table.

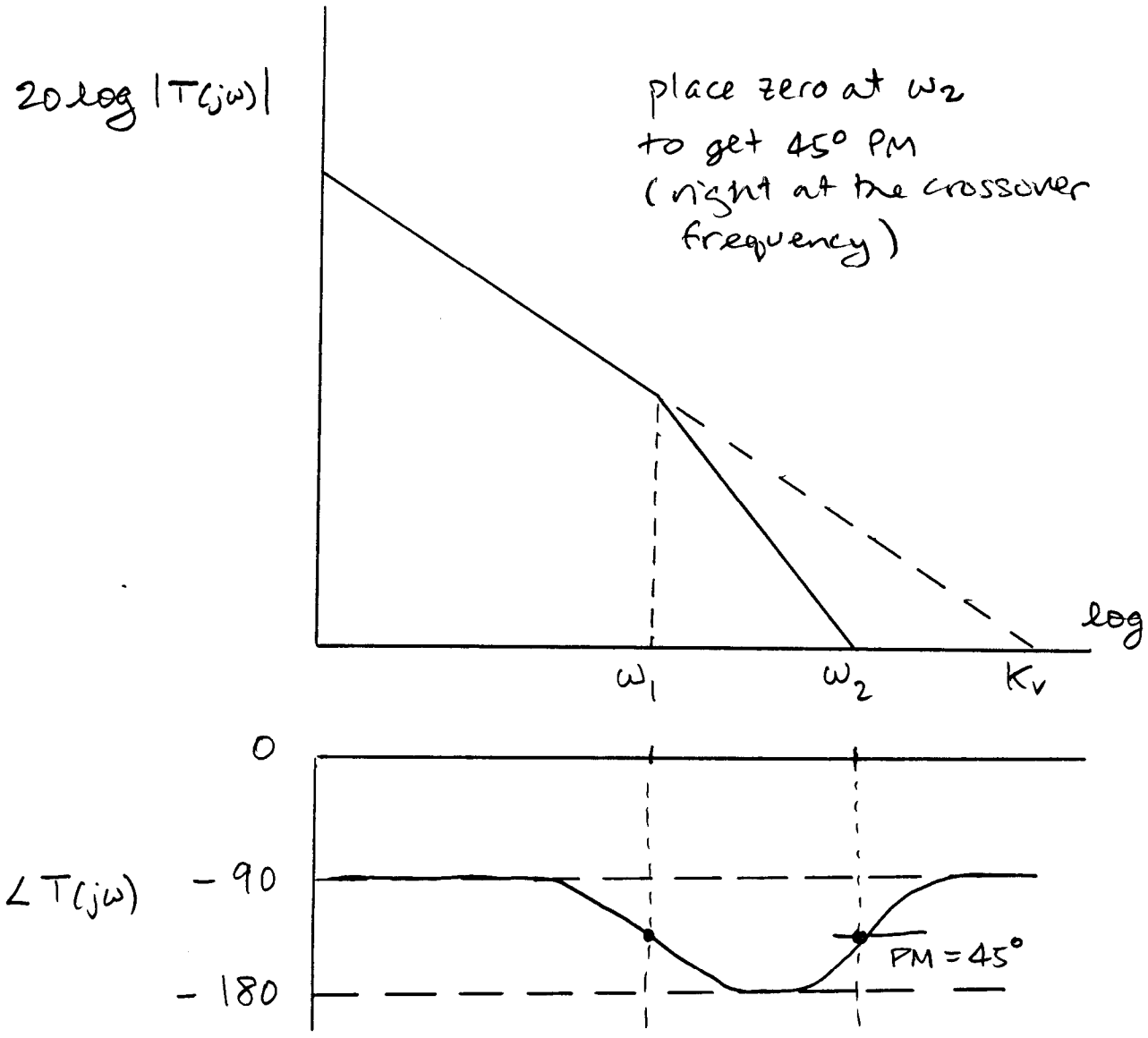
Bandwidth: (second-order with zero)

$$\omega_h = \omega_n\left[1 + 2\zeta^2 + \sqrt{(2\zeta^2+1)^2+1}\,\right]^{1/2}$$

$$\cong 2\omega_n \quad \text{for } \zeta = \frac{1}{\sqrt{2}}$$



You could also use a Bode plot to find the crossover frequency and phase margin


20 log |T(jω)|
place zero at ω2
to get 45° PM
(right at the crossover
frequency)
log
ω1
ω2
Kv
0
∠T(jω)
- 90
- 180
PM = 45°

F.M. Gardner, Phaselock Techniques, Wiley 1979.

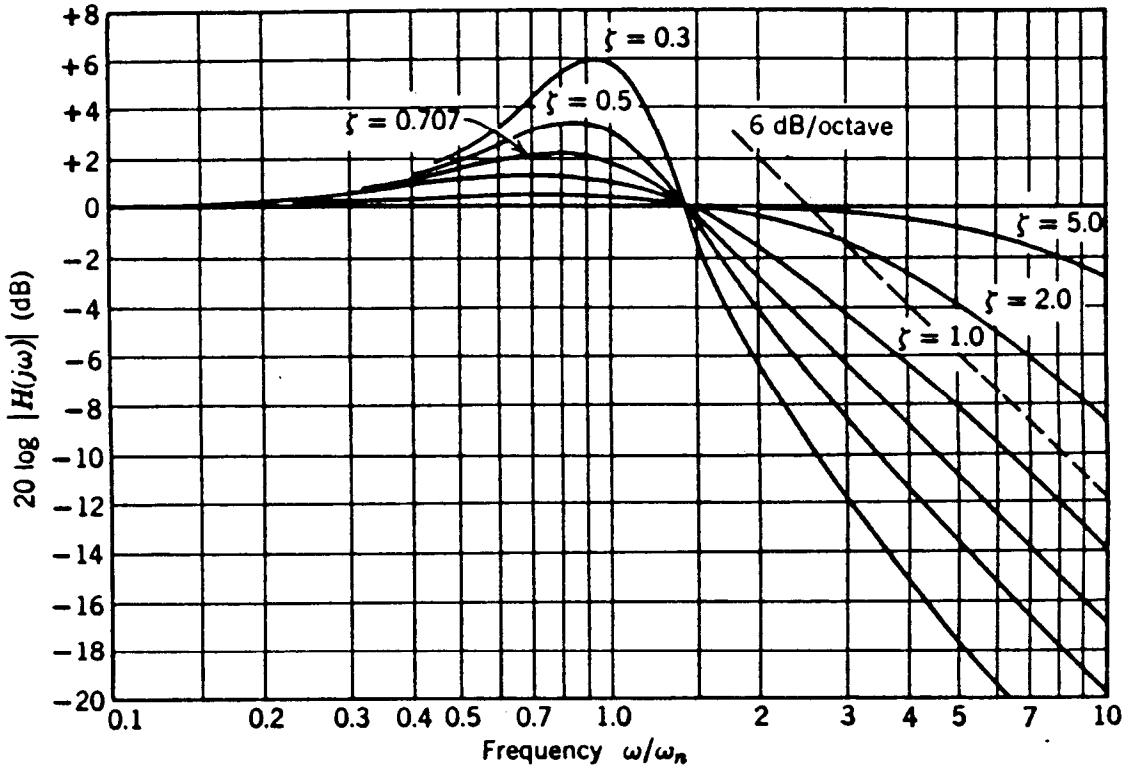


Figure 2.3 Frequency response of a high-gain second-order loop.

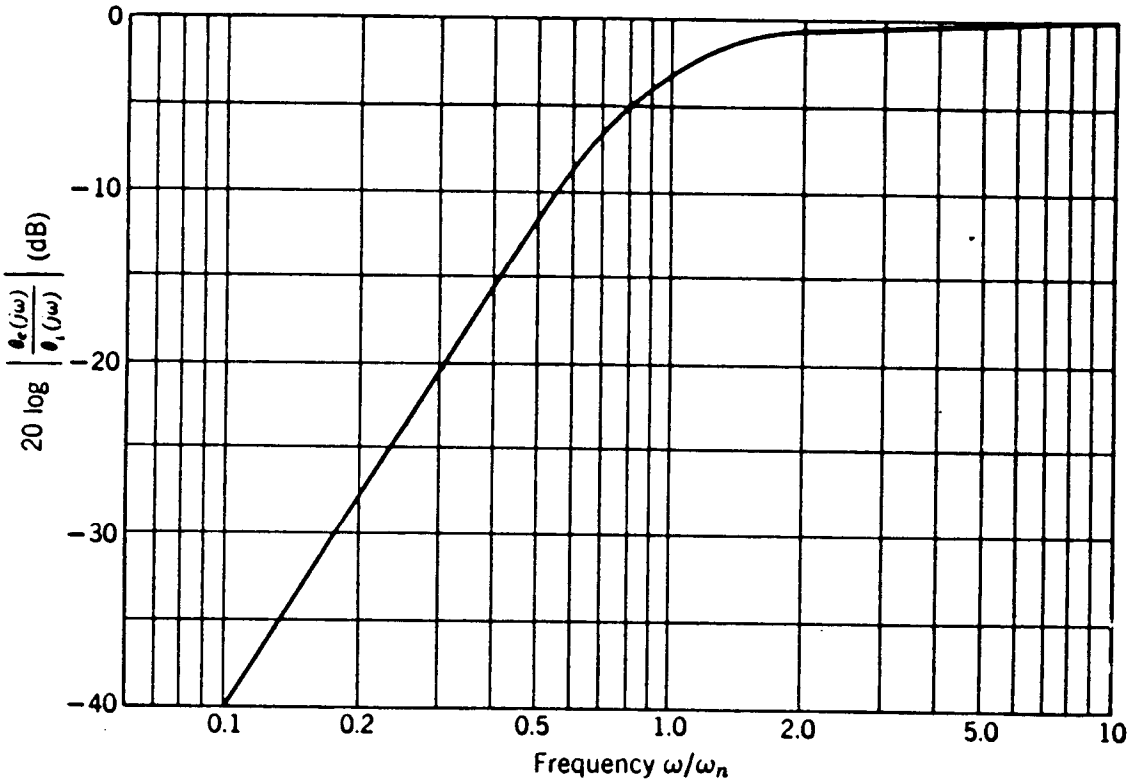


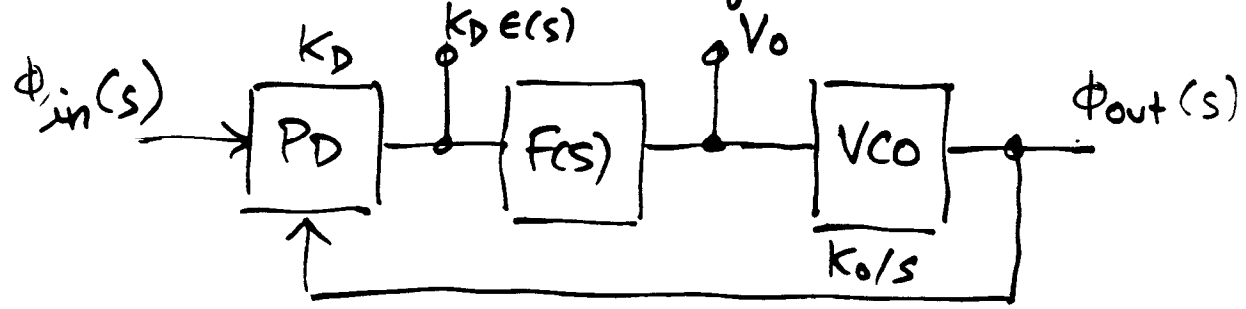
Figure 2.4 Error response of high-gain loop, $\zeta = 0.707$.

Phase Error

1. No freq. error when Loop is Locked

$$\omega_{osc} = \omega_i$$

2. Phase error can occur for certain θ_{in} conditions. Must remain bounded to keep Loop Locked.



$$\epsilon(s) = \phi_{in}(s) - \phi_{out}(s) = \frac{\phi_{in}(s)}{1 + T(s)}$$

3. Steady State Phase Error

$$\epsilon_{ss}(t \to \infty) = \lim_{s \to 0} s\, \epsilon(s)$$

4. Transient Phase Error

Use inverse Laplace Transform

We want to use the second-order, passive pole-zero filter due to its flexibility in choosing bandwidth and damping.

First, let's classify this filter.

$$T(s) = K_D F(s) K_0/s = \frac{K_D K_0 (1 + s/\omega_2)}{s (1 + s/\omega_1)}$$

TYPE = 1 because ↗ has exponent = 1

Now evaluate the DC phase error:

Phase Step. $\phi_{in}(s) = \frac{\Delta\theta}{s}$ (since $\phi_{in}(t) = \Delta\theta u($

$$\epsilon_{ss} = \lim_{s \to 0} \frac{s \cdot \frac{\Delta\theta}{s}}{1 + \frac{K_V}{s}\left(\frac{1 + s/\omega_2}{1 + s/\omega_1}\right)} = 0$$

No steady-state phase error for a phase step

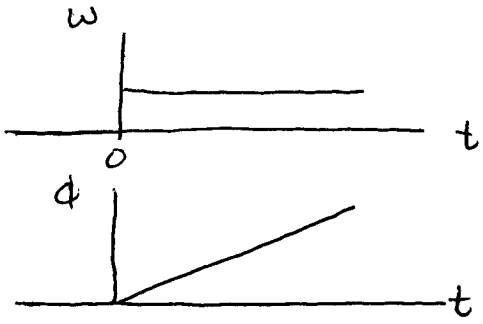
Frequency Step. $\phi_{in}(s) = \frac{\Delta\omega}{s^2}$ (phase ramp)

This is FSK modulation

input signal in time domain is

$$V_{in}(t) = V_{in} \sin(\omega_0 t + \Delta\omega t) \quad \text{at } t \geq 0^+$$

so $\phi = \Delta\omega t$



$$\epsilon_{ss} = \lim_{s\to 0} \frac{s\,\frac{\Delta\omega}{s^2}}{1 + \frac{K_D K_0}{s}\left(\frac{1+s/\omega_2}{1+s/\omega_1}\right)}$$

$$= \lim_{s\to 0} \frac{\Delta\omega}{s + K_0 K_D\left(\frac{1+s/\omega_2}{1+s/\omega_1}\right)} = \frac{\Delta\omega}{K_0 K_D F(0)}$$

there is an error, but it can be made small if $K_V = K_0 K_D$ is large.

Steady State Phase Error

Type 1; second order: $$F(s)=\frac{1+s/\omega_2}{1+s/\omega_1}$$

Input	$\phi_{in}(s)$	ε_{ss}
Phase step	$\Delta\theta/s$	0
Freq. step	$\Delta\omega/s^2$	$\Delta\omega/[K_O K_D F(0)]$
Freq. ramp	A/s^3	infinite

Type 2; second order: $$F(s)=\frac{s+a}{s}$$

Input	$\phi_{in}(s)$	ε_{ss}
Phase step	$\Delta\theta/s$	0
Freq. step	$\Delta\omega/s^2$	0
Freq. ramp	A/s^3	kA

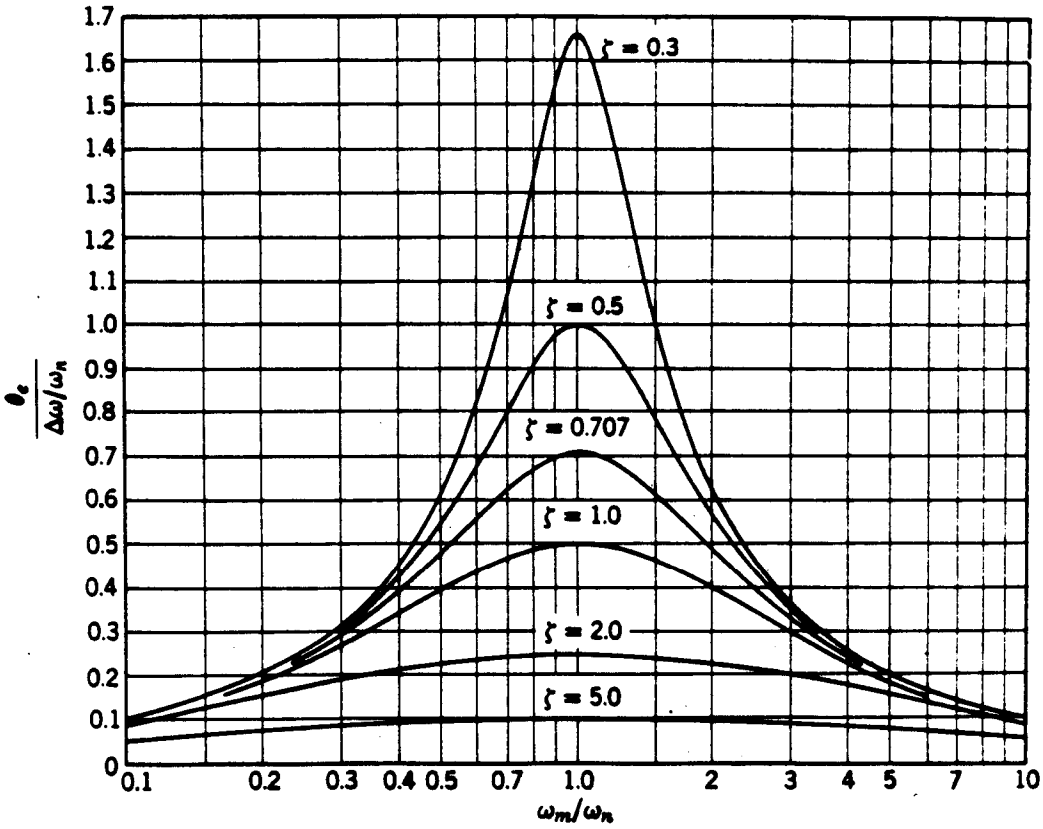


Figure 4-1 Steady-state peak phase error due to sinusoidal FM. (High-gain, second-order loop.) By permission of L. A. Hoffman.

Ref. F. M. Gardner, Phaselock Techniques

- For a sinusoidal FM source with frequency of modulation ω_m and deviation $\Delta\omega$, we see that the phase error can be kept small if ω_m/ω_n is small and K_v is large.

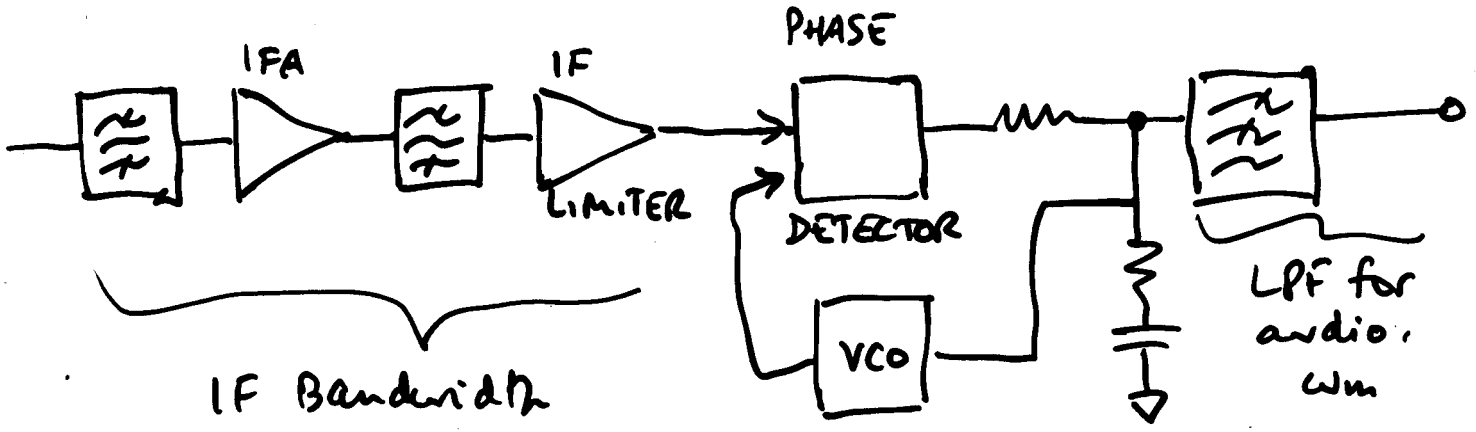
- For flat frequency response, we will choose $\zeta = \frac{1}{\sqrt{2}} = 0.707$

- In an FM broadcast receiver application, the channel bandwidth is limited to 200 kHz.

$$\omega_{m,max} = 15\,kHz$$

$$\Delta\omega_{,max} = 75\,kHz$$

Receiver For Sinusoidal FM Signal



IF Bandwidth

use Carson's Rule

$B \cong 2(\Delta\omega + \omega_m)$

$\omega_n \gg \omega_m$

$\zeta = 0.707$

Design Considerations for FM Demod PLL

1. Determine $K_V = K_D K_O F(0)$

This determines the locking range* and other filter parameters are derived from K_V.

$$\Delta\omega_L = \pm K_V \frac{\pi}{2}$$

The K_V is adjustable on the NE564 chip with a bias current.

From app note:

$$K_O = 5.9\, f_o \quad @ \quad I_{bias} = 0$$

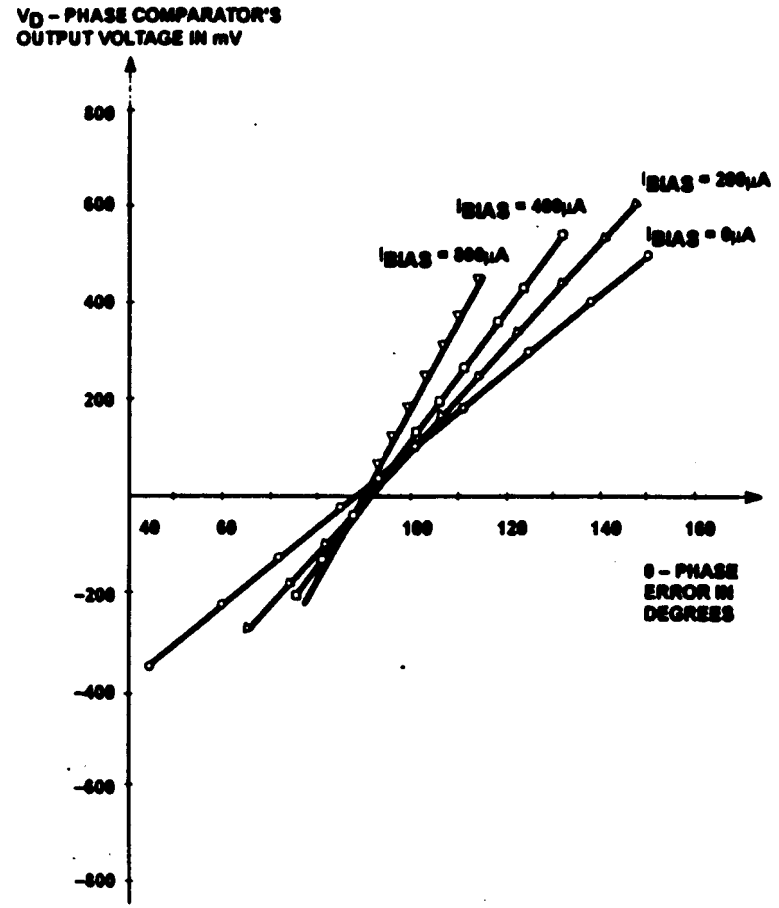
$$= 10.45\, f_o \quad @ \quad 800\mu A$$

$$K_D = \left[0.66 \frac{V}{rad} + 9.2 \times 10^{-4}\, I_{bias}(\mu A) \frac{V}{rad} \right]$$

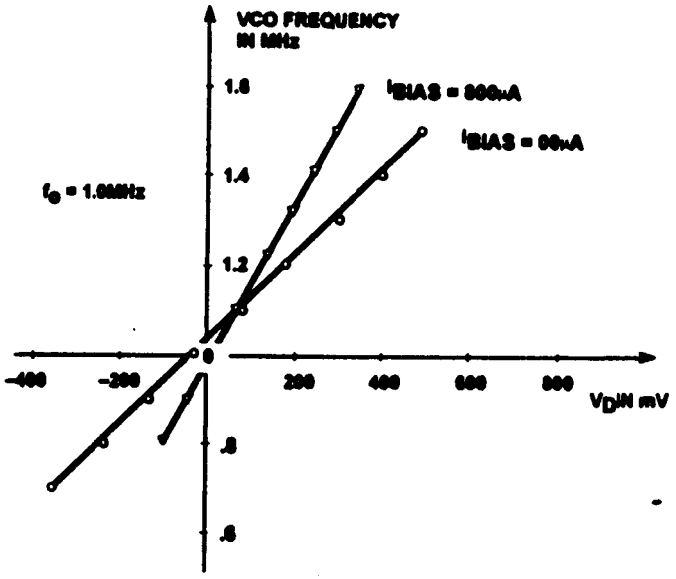
$-$

* on the NE564, the locking range is much smaller than predicted by $\Delta\omega_L$ — presumably limited by the VCO tuning range instead of the phase detector

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Variation of the Comparator's Output Voltage vs Phase Error and Bias Current (K_D)



VCO Output Frequency as a Function of Input Voltage and Bias Current (K_O)

2. with $\zeta = 0.707$ and

$$\omega_n = \sqrt{K_v \omega_1} \quad >> \omega_m$$

determine ω_1 and ω_2.

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_1}{K_v}} + \frac{1}{2}\frac{\omega_n}{\omega_2}$$

if K_v is large, the first term is small and can be neglected because $K_v >> \omega_1$ in this case.

For FSK, we have a frequency step. Must examine the transient phase error for an input phase ramp: $\theta_{in}(s) = \frac{\Delta\omega}{s^2}$

We see that the transient error peaks and greatly exceeds the steady state error.

Can the transient error pull the loop out of lock? One calculation showed that

$\Delta\omega_{po}$ = pull-out frequency step size

$= 1.8\,\omega_n(\zeta+1)$

(for second order loop)

If the loop pulls out of lock, it will skip cycles, then recapture the signal. But, we want square wave output.

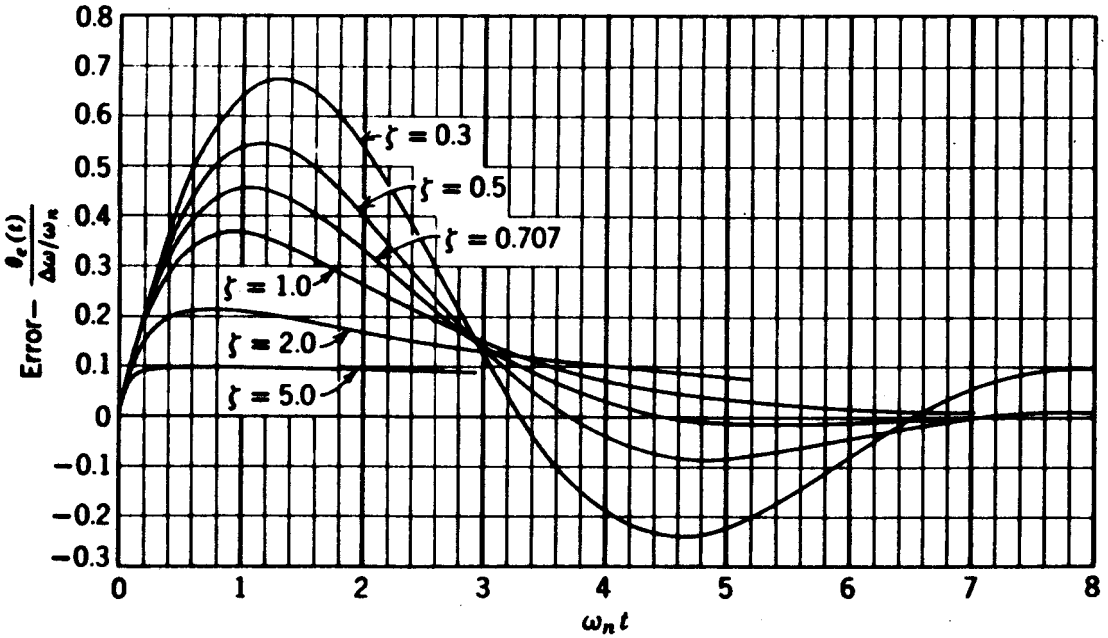
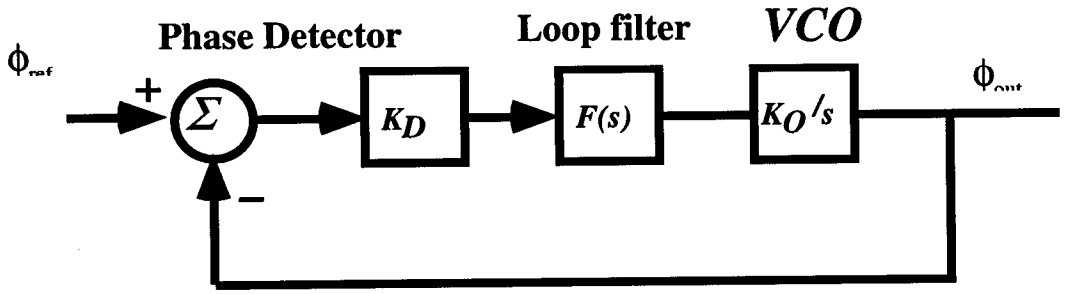


Figure 4-3 Transient phase error $\theta_e(t)$ due to a step in frequency $\Delta\omega$. (Steady-state velocity error, $\Delta\omega/K_v$, neglected.)
By permission of L. A. Hoffman.

Ref. F.M. Gardner, Phaselock Techniques

Frequency Synthesis – PLL

Reading: Motorola AN 535 and Manassewitsch (both in reading supplement)
Lee, Sect. 16.7



A phase locked loop is a feedback system that includes a VCO, phase detector, and low pass filter within its loop. Its purpose is to replicate the input frequency and phase on the output of the VCO when in lock. The phase detector produces an error voltage in proportion to the phase difference between the reference and VCO signals.

Frequency synthesizers use a PLL to copy, multiply, or divide a crystal reference source. The stability and phase noise properties of the crystal reference oscillator are preserved within the loop bandwidth of the PLL.

ϕ_{ref} = input reference phase.
- Usually from a crystal oscillator.

ϕ_{out} = output phase from VCO

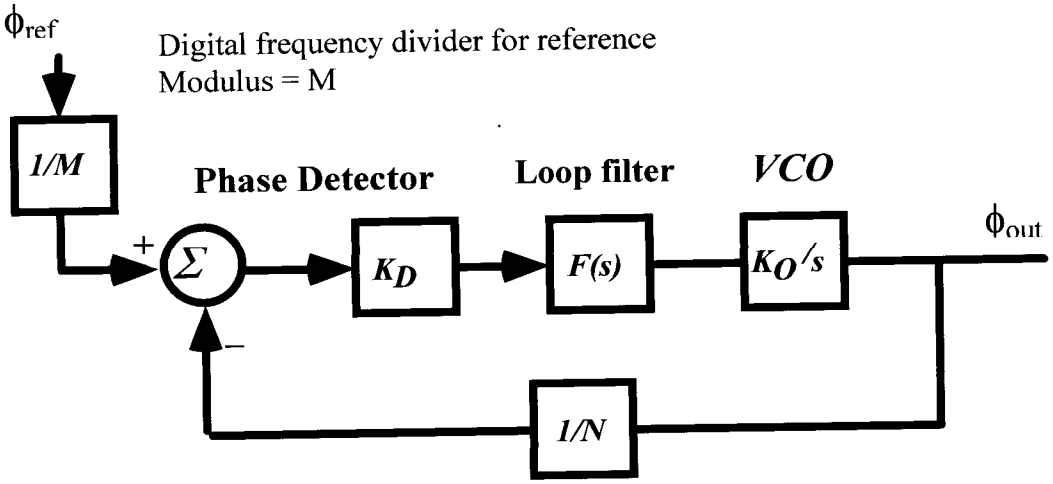
$\phi_{out} = \phi_{ref} + \text{const.}$
- Output phase is tracking input phase when loop is locked.

$\omega_{out} = \omega_{ref}$

- Output and input frequencies are the same when feedback factor = 1.

Loop filter: stabilizes loop. Establishes bandwidth of PLL and controls pull-in time required for loop to stabilize after a frequency change.

An output frequency that is a multiple of the reference frequency can be obtained if digital frequency dividers are included in the reference and VCO feedback path. The phase detector will keep the frequencies equal at its inputs and track the phases.



The output frequency is adjustable using digital variable modulus frequency dividers on the reference and VCO paths to the phase detector.

$$f_{out} = f_{ref} N/M$$

Thus, a tunable frequency source is available which has phase locked to a reference source and whose stability is similar to a fixed frequency crystal oscillator. For this structure, the frequency step size is f_{ref}/M.

How does the design of the frequency synthesizer differ from the FM Demodulator?

	FMD	FS
Input level	Can have low S/N	You choose the S/N for best performance. Crystal oscillator may have 100 dB S/N
Function	Tracking of frequency	Frequency up/down conversion
We want	Low THD Low noise	Low phase noise
Loop BW	Narrow – similar to IF bandwidth	As wide as possible while preserving low spurious outputs
Transfer function	$V_O(s)/\omega_{in}(s)$	$\phi_{out}(s)/\phi_{in}(s)$

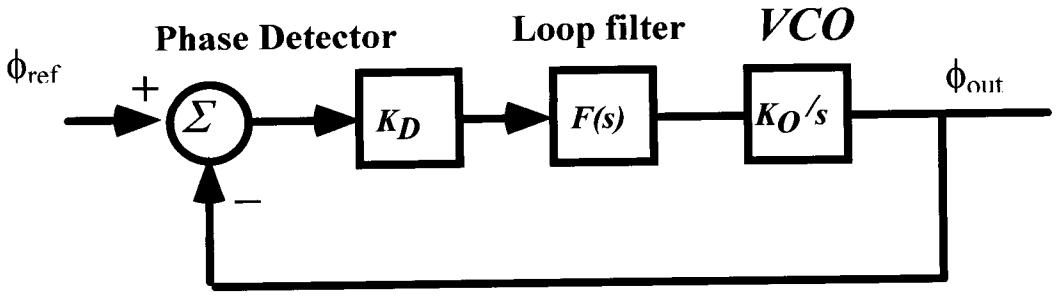
The frequency synthesis application is concerned with:

1. Transient response to a frequency step
2. Steady state phase error for frequency step
3. Stability of feedback loop
4. Phase noise and timing jitter

We will first examine the loop filter design to see how it may affect 1 – 3.

Steady State Error. A characteristic of feedback control systems. This is the error remaining in the loop at the comparator output after all transients have died out. In the case of the frequency synthesizer, it is the output from the phase detector, $\phi_{ref} - \phi_{out}$ that constitutes the error, ε.

First we will consider the FS with feedback = 1; therefore, input and output frequencies are identical.



Transfer Function: H(s) = forward path gain / [1 + T(s)].

With feedback = 1,

$$H(s) = T(s)/[1 + T(s)]$$

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(s)}{s + K_D K_O F(s)}$$

Phase error function:

$$\varepsilon(s) = \phi_{ref} - \phi_{out} = \frac{s\phi_{ref}}{s + K_D K_O F(s)}$$

For the frequency synthesis application, we want to have ideally perfect phase tracking for phase and frequency steps. When the synthesizer frequency is changed, it is a discontinuous step in modulus, and we want to have zero steady state phase error in this case.

In the phase error analysis for the type 1 passive pole-zero lag filter, we found that there was a static phase error for a frequency step. To eliminate this phase error, we need a TYPE = 2 loop gain function. That is, the s factor in the denominator must have an exponent of 2.

Placing an opamp RC integrator in the loop will give

$$F(s) = \frac{s + a}{s}$$

where the zero at a = ω_2 in the FMD discussion. Then, the loop gain T(s) will be that of a type 2 control system:

$$T(s) = \frac{K_D K_O (s + a)}{s^2}$$

Steady State Phase Error

Type 1; second order: $$F(s)=\frac{1+s/\omega_2}{1+s/\omega_1}$$

Input	$\phi_{ref}(s)$	ε_{ss}
Phase step	$\Delta\theta/s$	0
Freq. step	$\Delta\omega/s^2$	$\Delta\omega/[K_O K_D F(0)]$
Freq. ramp	A/s^3	infinite

Type 2; second order: $$F(s)=\frac{s+a}{s}$$

Input	$\phi_{ref}(s)$	ε_{ss}
Phase step	$\Delta\theta/s$	0
Freq. step	$\Delta\omega/s^2$	0
Freq. ramp	A/s^3	kA

Now find the closed loop transfer function by inserting F(s):

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(s)}{s + K_D K_O F(s)}$$

$$H(s) = \frac{(1 + s/a)}{\frac{s^2}{K_D K_O a} + \frac{s}{a} + 1}$$

Thus, we can see that

$$\omega_n = \sqrt{K_D K_O a}$$

$$\varsigma = \frac{\omega_n}{2a}$$

These parameters will have a strong effect on the loop dynamics which control overshoot and settling time. From the system design perspective, overshoot can be quite harmful, since it will cause the frequency to temporarily exceed the steady state value. Thus, the output of the synthesizer might land in an adjacent channel during part of the transient response. Settling time can also be critical since many TDM applications use different receive and transmit frequencies. The settling time determines how long you must wait until transmitting or receiving after a hop in frequency.

Bandwidth: The loop 3 dB bandwidth is important for noise considerations. It is determined by ω_n and ζ, so bandwidth must be determined in conjunction with the overshoot and settling time specifications.

$$\omega_h = \omega_{3dB} = \omega_n \left[1 + 2\zeta^2 + \sqrt{(2\zeta^2 + 1) + 1} \right]^{1/2}$$

Noise bandwidth: When PLL is used in a synthesizer application, the reference source noise is replicated within the noise bandwidth of the loop. While related to the 3 dB bandwidth, a more accurate calculation would use:

$$B_n = \frac{1}{2\pi} \int_0^\infty \left| \frac{\phi_{out}}{\phi_{in}} \right| d\omega$$

Outside the noise bandwidth, the VCO noise spectrum dominates. Within the bandwidth, the loop gain suppresses the VCO noise. The loop acts as a low pass filter for reference noise and a high pass filter for VCO noise.

Synthesizer Settling time problem

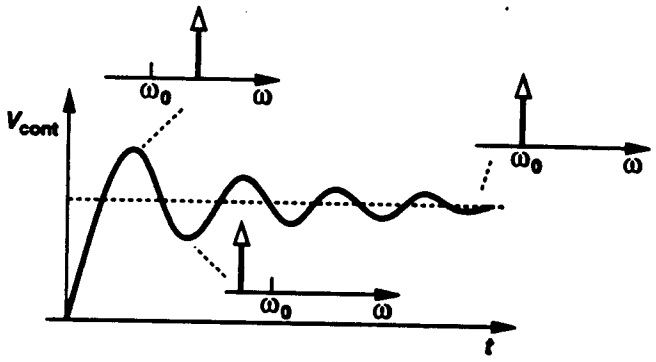


Figure 8.33 Variation of VCO frequency during synthesizer settling.

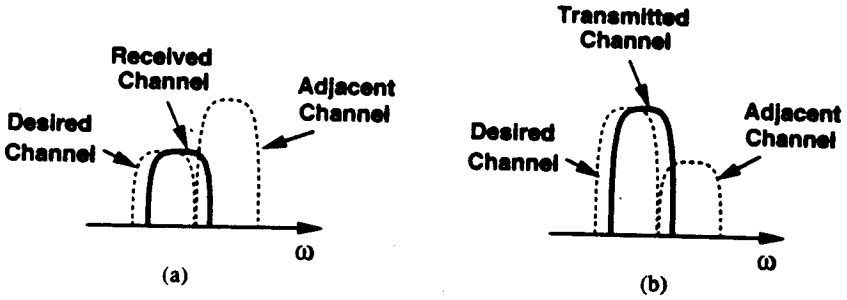


Figure 8.34 Effect of synthesizer settling on received and transmitted channels.

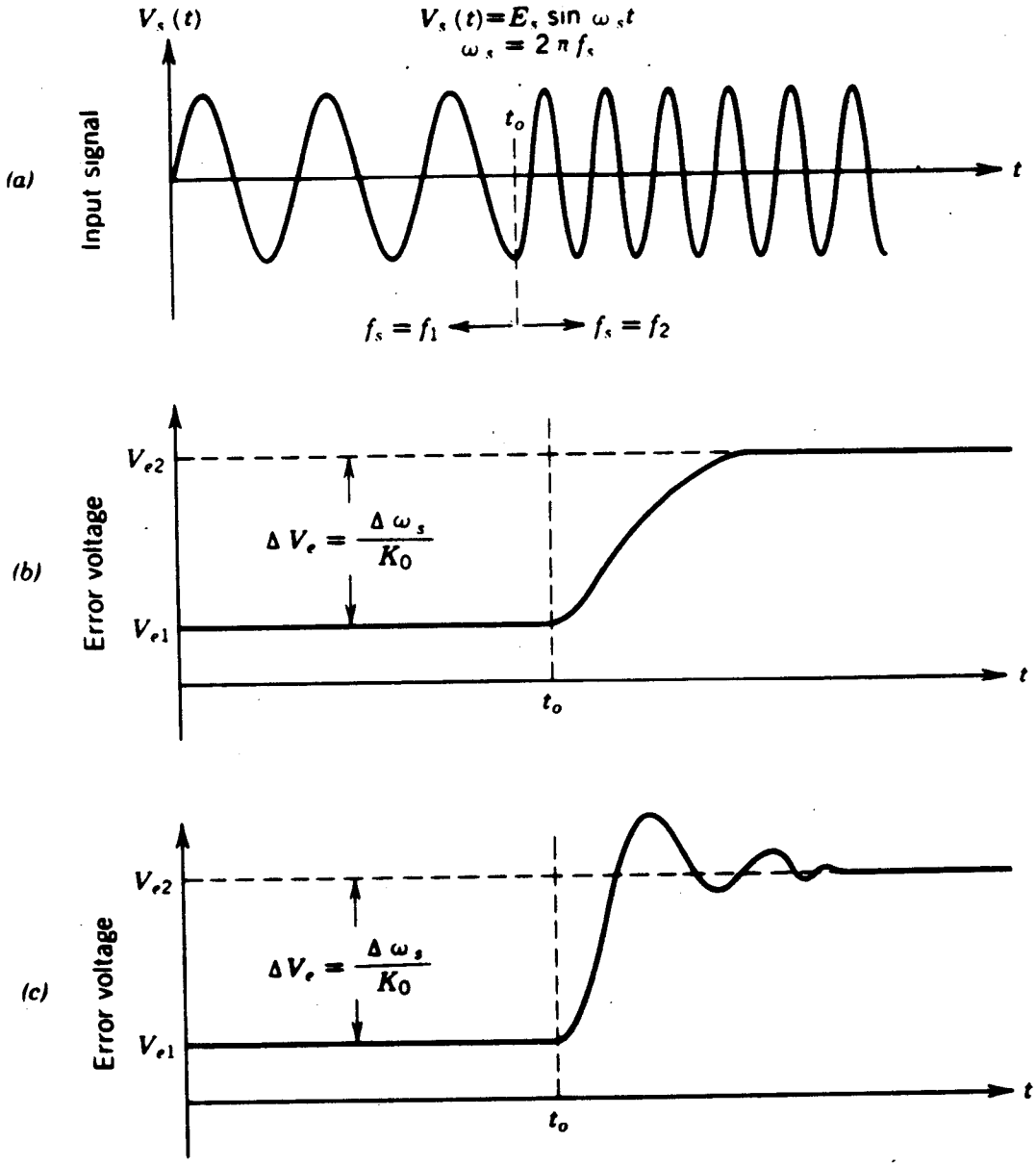


FIGURE 12.8. Transient response of PLL to step change of input frequency: (*a*) Input signal; (*b*) step response of overdamped loop ($\zeta > 1.0$); (*c*) step response of underdamped loop ($\zeta < 1.0$).

Suppose modulus changes from M to M+k.

Calculate time required for four to be within $(1 \pm \alpha)(M+k) f_{REF}$

α = settling accuracy

It can be shown that

$$t_s \approx \frac{1}{\zeta \omega_n} \ln\left\{\frac{k}{M|x|\sqrt{1-\zeta^2}}\right\}$$

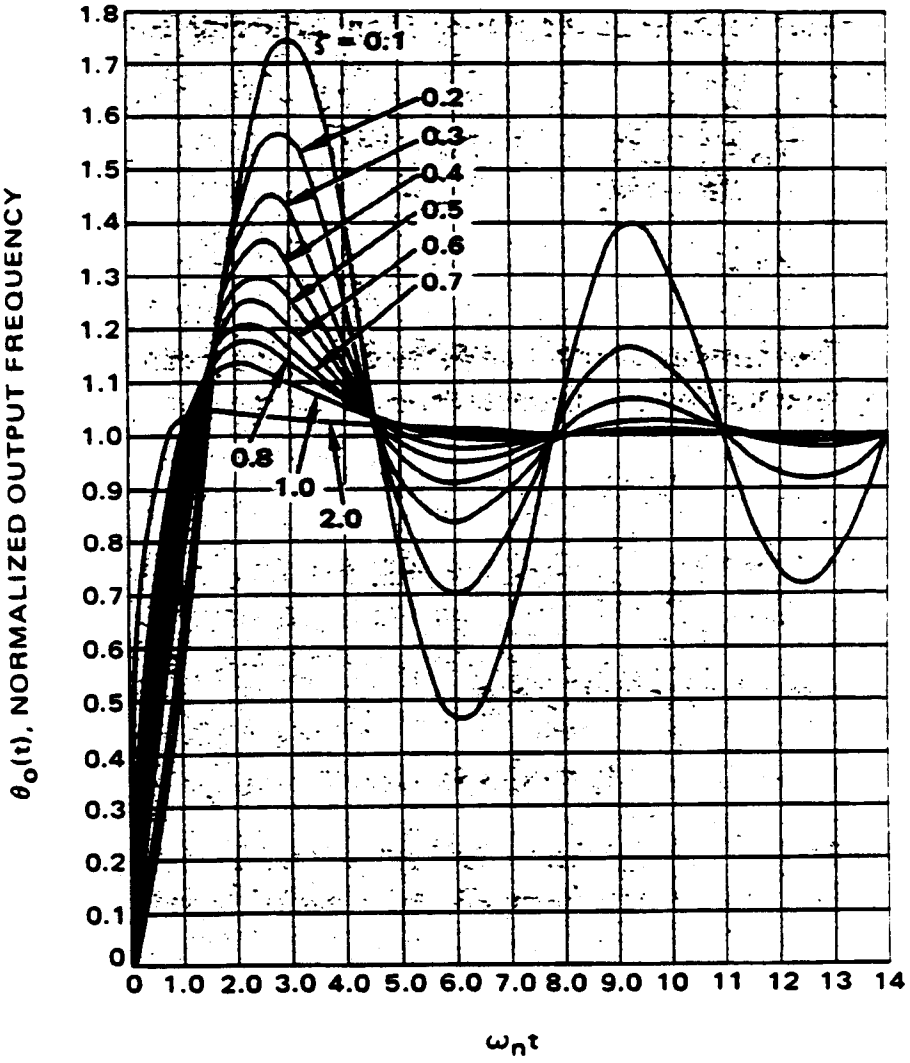
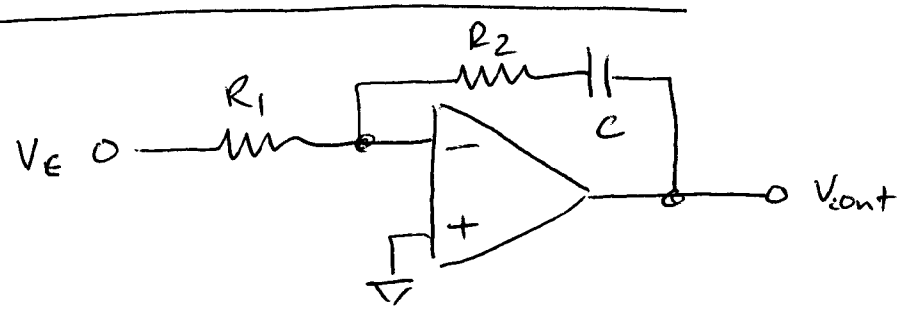


FIGURE 6 — Type 2 Second Order Step Response

From: Motorola AN 535

Filter Implementation



$$\frac{V_{cont}(s)}{V_E} = \frac{1 + sR_2C}{sR_1C} = F(s)$$

behaves as ideal integrator plus provides the zero.

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{(1 + sR_2C)}{s^2\left(\frac{R_1C}{K_V}\right) + R_2Cs + 1}$$

$$K_V = K_D K_O$$

$$\omega_n = \sqrt{\frac{K_V}{R_1C}}$$

$$\frac{2\zeta}{\omega_n} = R_2C \; ; \quad \zeta = \frac{R_2C\omega_n}{2}$$

Stability

Examine root-locus or determine phase margin.

Loop Gain:

$$T(s) = K_V \left(\frac{1 + sR_2C}{s^2 R_1 C} \right)$$

$$1 + T(s) = s^2 + K_V \frac{R_2}{R_1} s + \frac{K_V}{R_1 C} = 0$$

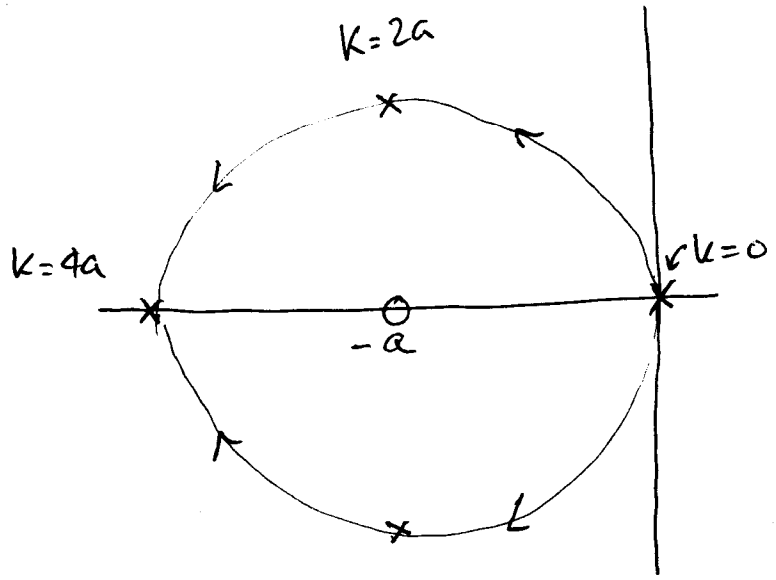
let $K = K_V \frac{R_2}{R_1}$ $\qquad a = R_2 C$

$$s^2 + Ks + Ka = 0$$

$$s = -\frac{K}{2} \pm \frac{1}{2} \sqrt{K^2 - 4Ka}$$

$K = 0$. here $s^2 = 0$

so both poles at origin



we see that the imaginary part will at first grow with K (as $K^2 << 4Ka$ for small K), will reach maximum, next will decrease and become real. The real part grows with K in negative direction.

Maximum imaginary component;

$$\frac{d}{dK}(K^2 - 4Ka) = 0$$

$K = 2a$. $\mathrm{Im}\{s\} = \pm\frac{1}{2}\sqrt{4a^2 - 8a^2} = \pm ja$

$\mathrm{Re}\{s\} = -a$

s becomes real. $k^2 - 4ka = 0$

$k = 4a$

$s = -2a$

Trajectory looks suspiciously like a circle!

Conclusion: Unconditionally Stable

Also, $\omega_n = \sqrt{ka}$ = natural frequency

$\zeta = \frac{1}{2}\sqrt{\frac{k}{a}}$ = damping factor

These have the same geometric interpretation as previously discussed with FMD application.

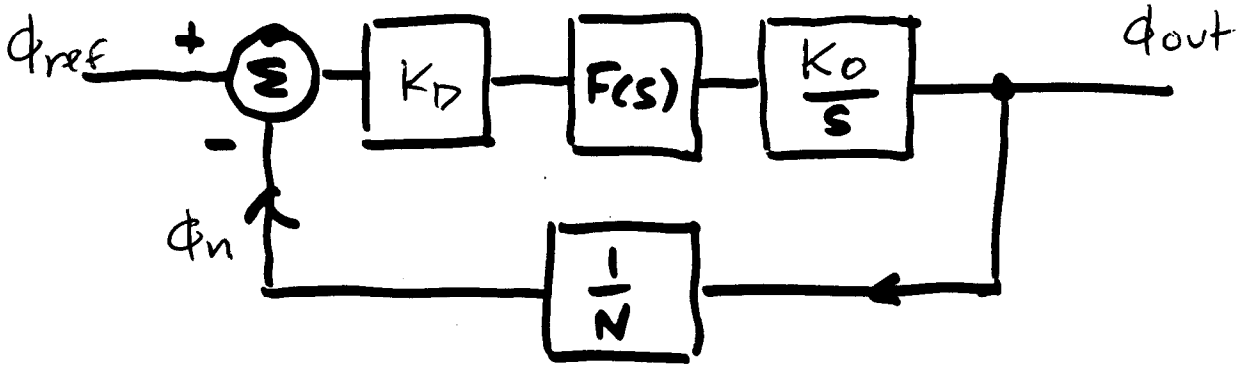
$\zeta = \cos\phi \quad (0 \le \phi \le \frac{\pi}{2})$

$k = 0, \quad \phi = \frac{\pi}{2}, \quad \zeta = 0$
totally undamped

$k = 2a, \quad \phi = \frac{\pi}{4}, \quad \zeta = 0.707$

$k = 4a, \quad \phi = 0, \quad \zeta = 1$

Synthesizer PLL



- Freq. divider used in feedback path

$$\frac{\phi_n}{\phi_{out}} = \frac{1}{N} \qquad N = \frac{\omega_{out}}{\omega_{ref}}$$

$$T(s) = \frac{K_D F(s) K_O}{Ns}$$

- Loop gain reduced by N
- N is not constant
- K_V is not constant

Let's design a synthesizer

We can start with a transient spec. for lock up of the PLL.

overshoot $< 20\%$

settling time $1\,ms$

From Fig. 6, we see $\zeta = 0.8$ meets overshoot spec. Settling occurs to within 5% at $\omega_n t = 4.5$ or 1% for $\omega_n t \cong 5.5$.

$$\text{so } \omega_n = \frac{4.5}{1\,ms}$$

$$\text{and } \omega_n = \sqrt{\frac{K_V}{R_1 C N}} \qquad K_V = K_D K_O$$

$$\zeta = \frac{R_2 C \omega_n}{2} = \frac{R_2}{2}\sqrt{\frac{K_V C}{R_1 N}}$$

Note that:

1. K_D is fixed. Depends on the phase detector

2. K_O is found from the slope of the VCO tuning curve, $d\omega_{out}/dV_{cont}$.

In general, this is not constant, but varies with tuning voltage.

3. N is determined by

$$N = \frac{\omega_{OUT}}{\omega_{ref}} = \frac{\omega_{OUT}}{\omega_{xtal}/R}$$

The change in N required to tune over the required range and the change in K_O causes the loop gain T to vary with frequency.

Since damping increases with K_V and decreases with $\sqrt{\frac{1}{N}}$, loop dynamics will depend on N.

4. The phase detector will have a maximum output current. R_1 must be consistent with V_{DD}/I_{max}. See data sheet

5. Choose C to determine ω_n.

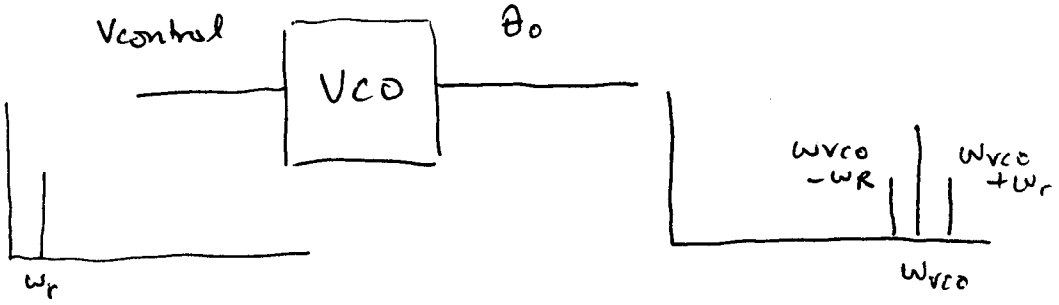
6. Use ζ to determine R_2.

An alternate design sequence could have used the loop bandwidth, $\omega_n = \omega_{3dB}$. We will show later that this is the phase noise corner frequency. From ω_{3dB} and ζ, ω_n could be determined. The settling time then is set by default.

Other design considerations.

Notice that the PFD output has a strong component at ω_R, the reference frequency.

With our type of PLL synthesizer, if we require small step size, then ω_R is small. The loop filter must attenuate ω_R otherwise the VCO will be modulated by the ac component on its control voltage.



Thus, we cannot "have our cake and eat it too".

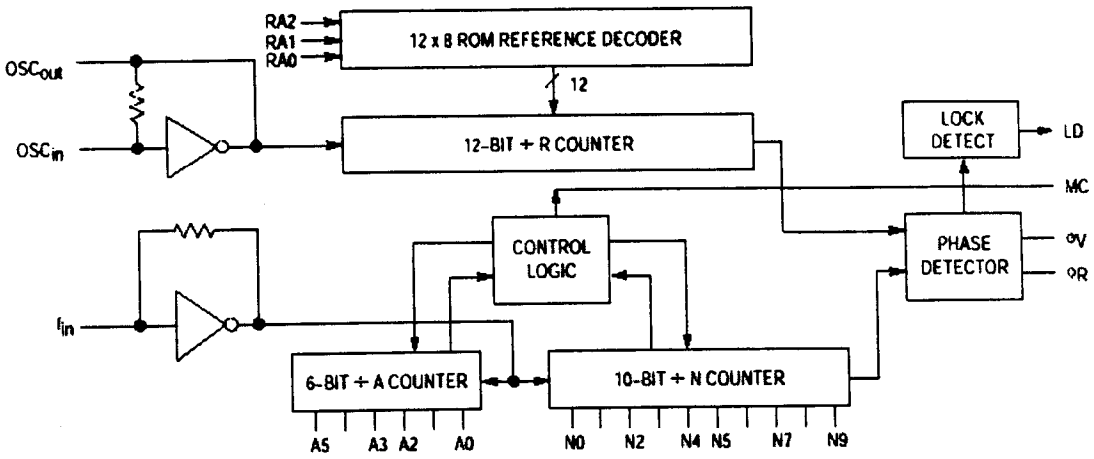
According to the data sheet,

$$\omega_n \cong \frac{\omega_R}{10}$$

so that the loop filter will adequately attenuate the ref frequency.. This will limit our ability to choose settling time and bandwidth.

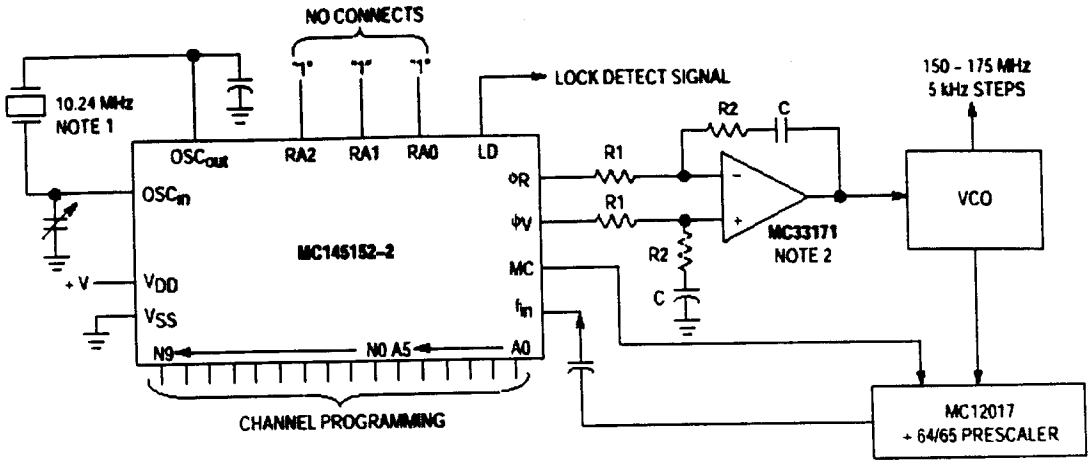
Motorola MC145152-2 Frequency Synthesizer

MC145152-2 BLOCK DIAGRAM



NOTE: N0 – N9, A0 – A5, and RA0 – RA2 have pull–up resistors that are not shown.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048



NOTES:
1. Off–chip oscillator optional.
2. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase–Locked Loop — Low–Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail–to–rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

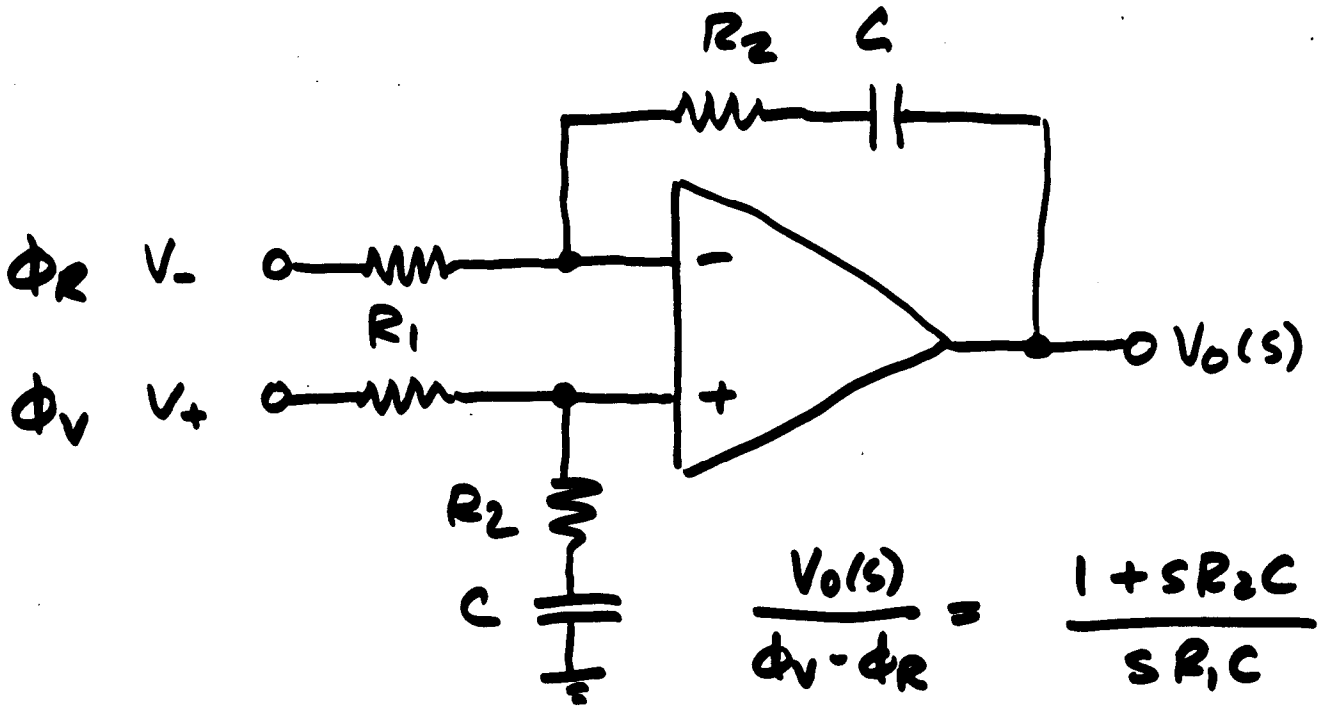
Figure 1. Synthesizer for Land Mobile Radio VHF Bands

A counter: MC = 0; divide by P+1
Counts down from A until A = 0 then

N counter: MC = 1; divide by P
Counts down from N-A to 0 then reset counters to initial values and start again.

$$N_{Total} = (N-A)P + A(P+1) = NP + A$$

Filter Implementation



$$\frac{V_o(s)}{\phi_V - \phi_R} = \frac{1 + sR_2C}{sR_1C}$$

Integer-N synthesizer.

f_{REF} = channel spacing.

Drawbacks:

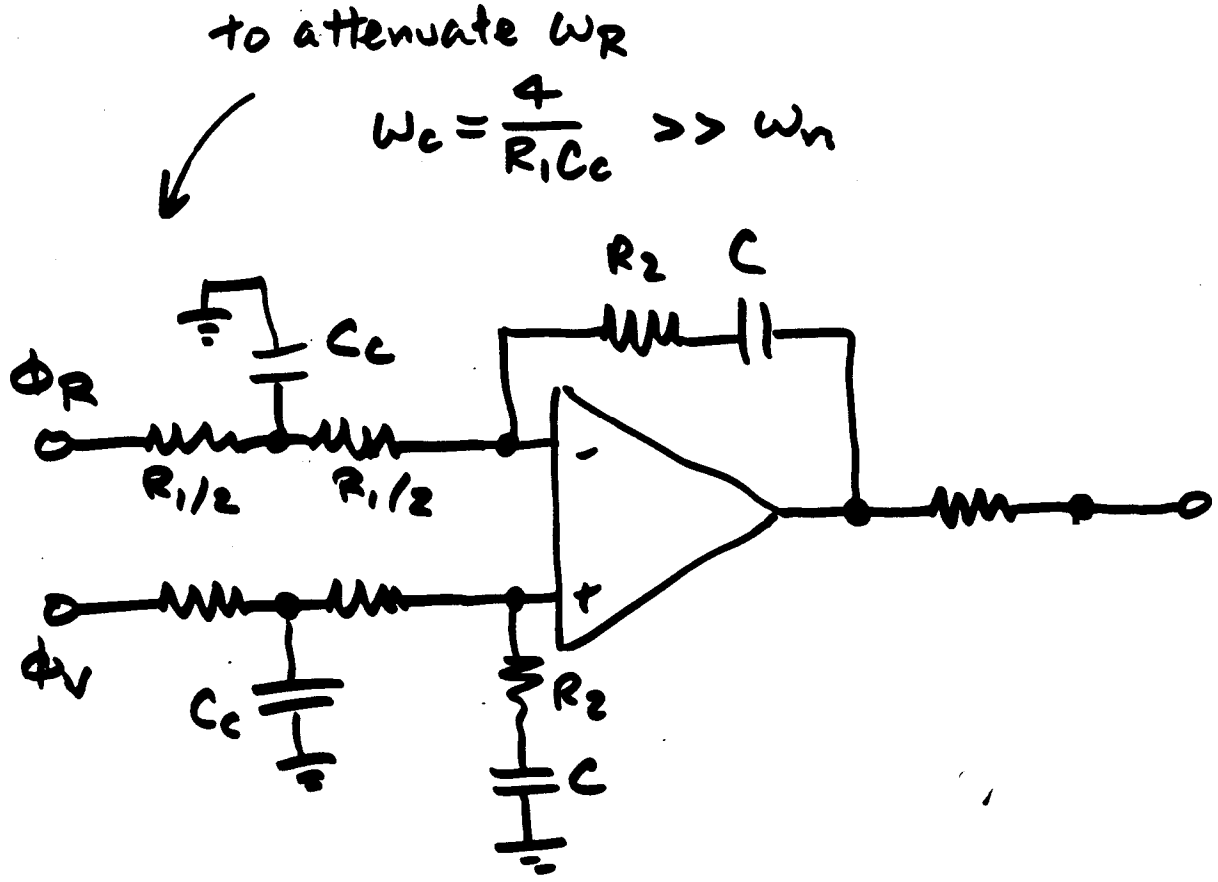
1. Reference spurs. Narrow channel spacing implies a low f_{REF}. Since PFD produces a strong output component at f_{REF}, loop filter must remove this. Otherwise reference sidebands will show up on output since VCO will be modulated by f_{REF}.

Extra filtering can be added.

Causes 3rd order loop. Becomes less stable unless pole introduced is much higher than the zero. In this case, it may not help much

Notch filter can be used. Series LC would have good rejection. But must be careful of how the phase is affected by it at freq. below f_{REF}.

Filter modifications



PHASE DETECTOR

Gilbert Multiplier is often used on ICs.

- compact
- low power
- conversion gain

$$\Delta I \cong I_{EE}\left(\frac{V_1}{2V_T}\right)\left(\frac{V_2}{2V_T}\right)$$

In phase detector application it is intentionally driven into switching mode of operation.

dc component:

$$V_{average} = \frac{1}{2\pi}\int_0^{2\pi} V_0(t)\, d(\omega_0 t)$$

$$= -\frac{1}{\pi}(A_1 - A_2)$$

$$= -\frac{I_{EE}R_C}{\pi}\left[(\pi-\phi)-\phi\right]$$

$$= I_{EE}R_C\left(\frac{2\phi}{\pi}-1\right)$$

XOR

A	B	Vout
0	0	0
0	1	1
1	0	1
1	1	0

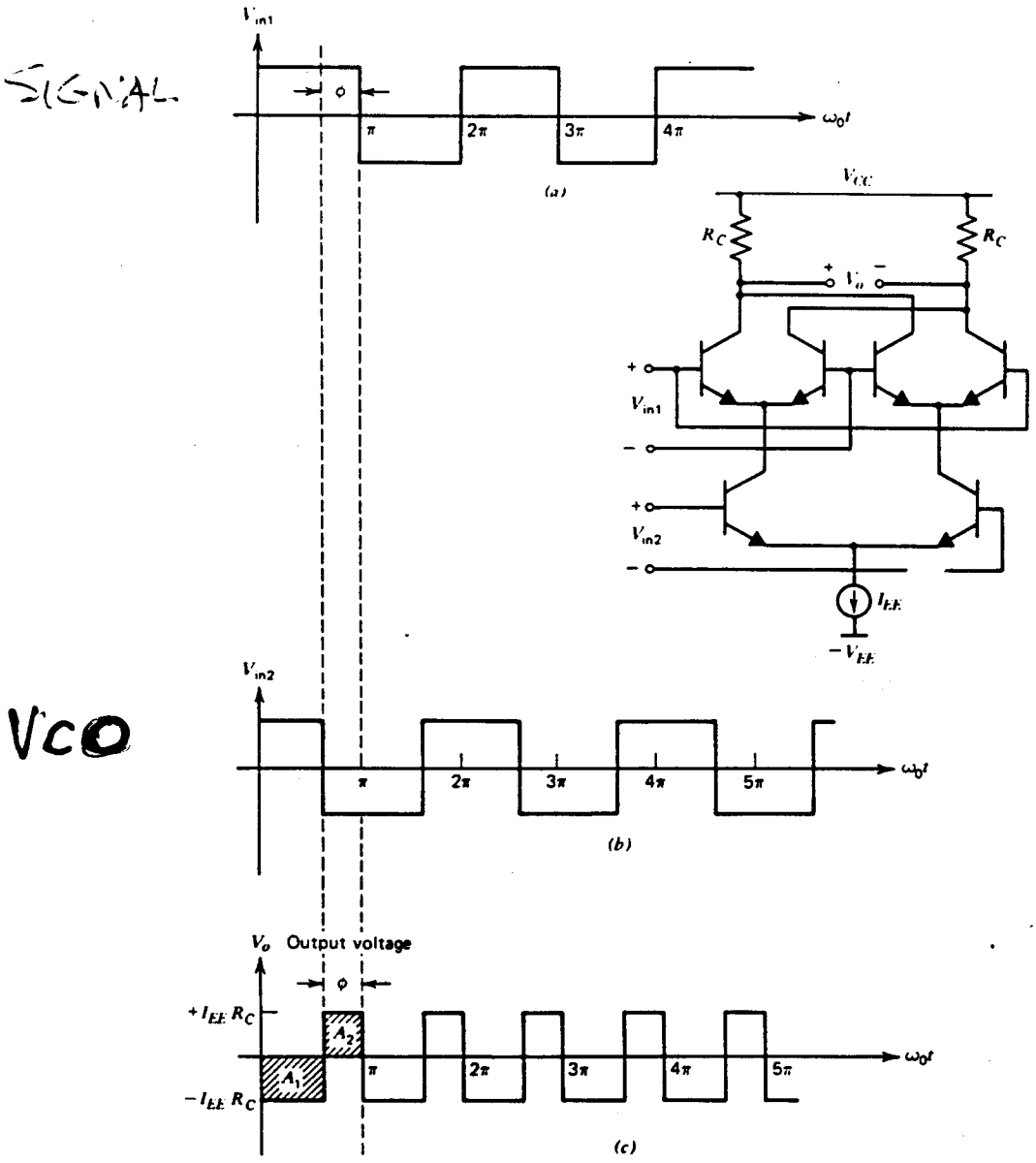


Figure 10.16 Typical input and output waveforms for a phase detector.

Gilbert/

XOR Phase Detector. switch or multiplier

1. Phase detector gain sensitive to duty cycle – should be 50%

2. 90° phase offset. midpoint is at $\phi = \frac{\pi}{2}$

3. 2x feedthrough

4. if $f_1 \neq f_2$, we get output at $f_1 \pm f_2$.

5. tolerant of signal dropout

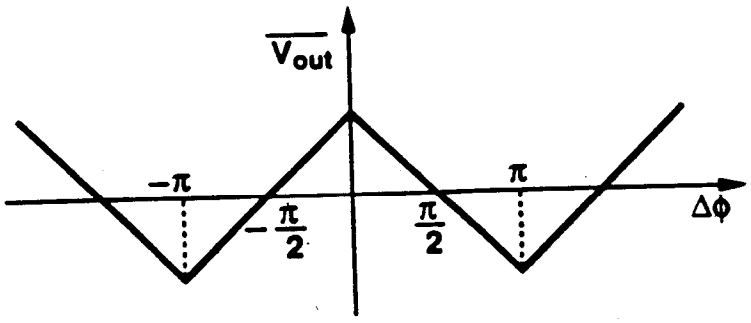
6. $K_D = \frac{2 I_{EE} R_C}{\pi}$ for Gilbert

$K_D = \frac{V_{DD}}{\pi}$ for XOR

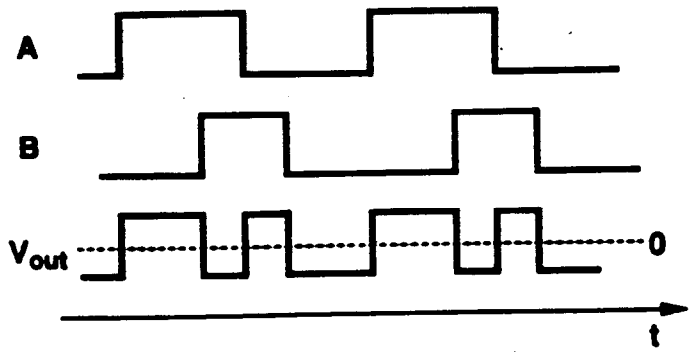
7. Not very fast when $f_1 \neq f_2$ since gain in metastable state is same gain as in stable operating point.

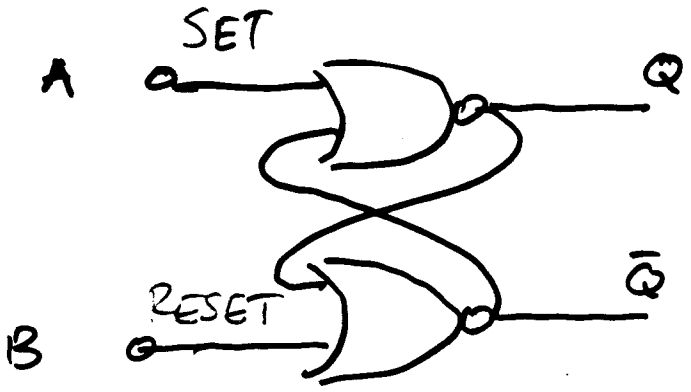
8. Can lock on harmonics. Suppose $\omega_{VCO} = 3\omega_{Ref}$. 3rd harmonic will be at VCO freq.

Averaged output of XOR/Gilbert phase detector

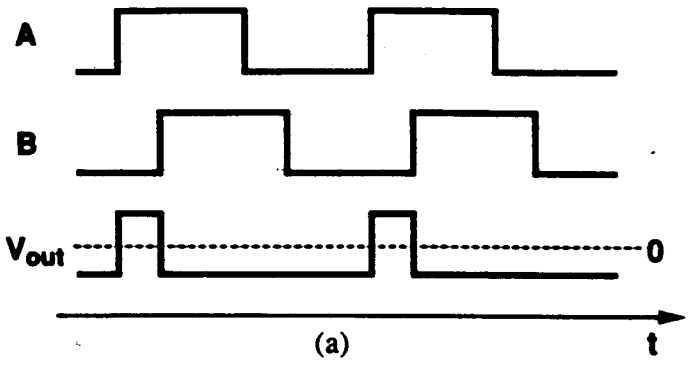


Duty cycle other than 50% will cause static phase error

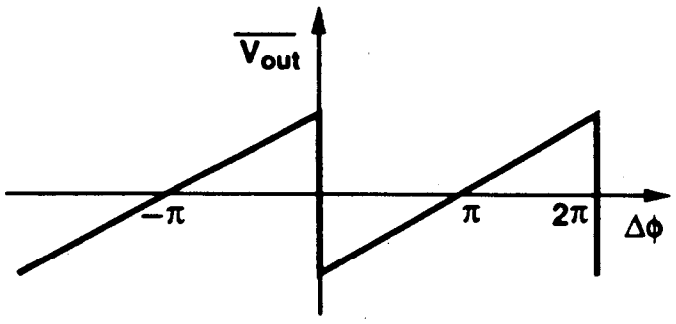



SET
A
Q
$\bar{Q}$
RESET
B


A
B
S
R
RS
Latch
Q
$\bar{Q}$
V_{out}


A
B
V_{out}
0
t

(a)


$\overline{V_{out}}$
$-\pi$
π
2π
$\Delta\phi$

(b)

RS Latch Phase Detector

1. Gain constant over 0 to 2π phase range.
   → doubled tracking range
2. Duty cycle independent
3. 180° = zero output.
4. Output is at f_R, not $2f_R$ → Loop Filter must have narrow bandwidth

Improvement over Gilbert PD, but still no frequency acquisition assistance to improve capture.

but - gain is very high in metastable state also, it can lock on harmonics. Limits applications in frequency synthesis.

$$K_D = \frac{V_{DD}}{2\pi}$$ single-ended

OUTPUT

or

$$\frac{V_{DD}}{\pi}$$ differential

PHASE - FREQUENCY DETECTOR

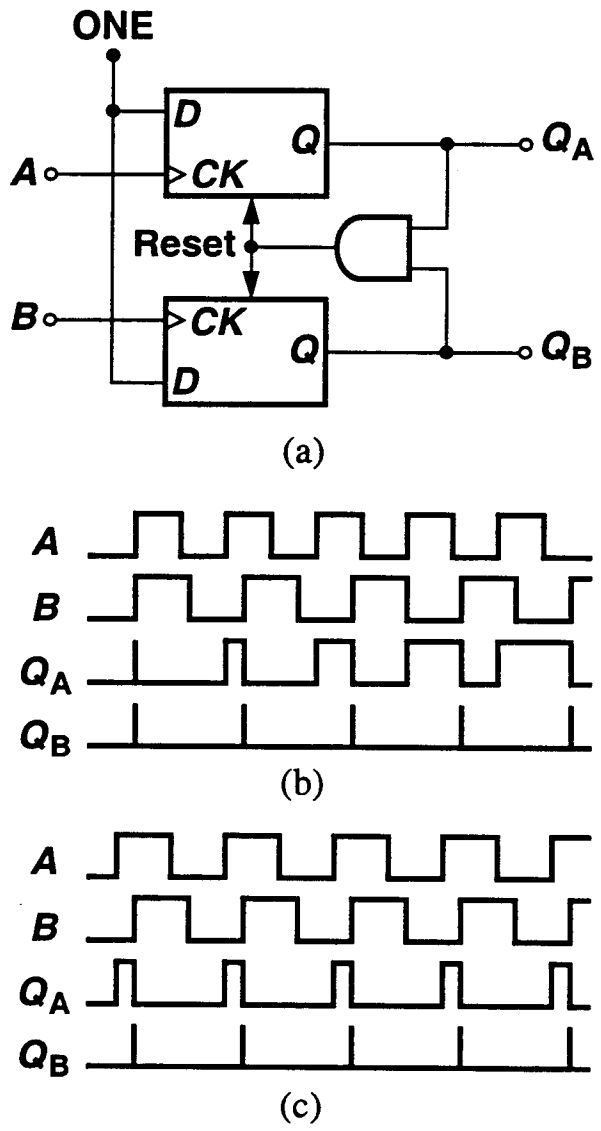
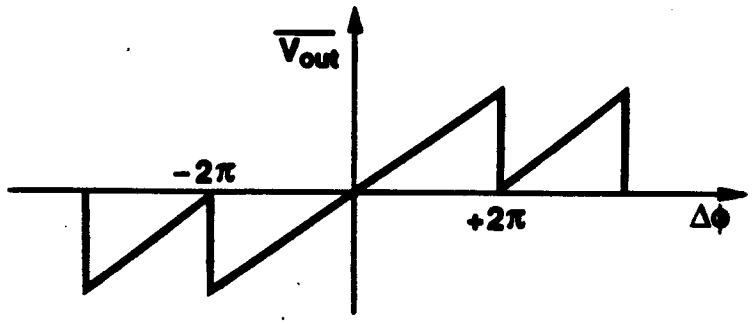


Figure 3.26. (a) Phase/frequency detector. Circuit response with (b) $\omega_A \geq \omega_B$, (A leading B.



$$K_D = \frac{V_{DD}}{2\pi}$$

Fig. 45 PFD charact

Pal Savir And Razavi High Speed CMOS Circuits

Digital Phase-Frequency Detector

1. Insensitive to duty cycle of inputs

2. Wider range -2π to $+2\pi$

3. Indicates polarity of freq. difference.

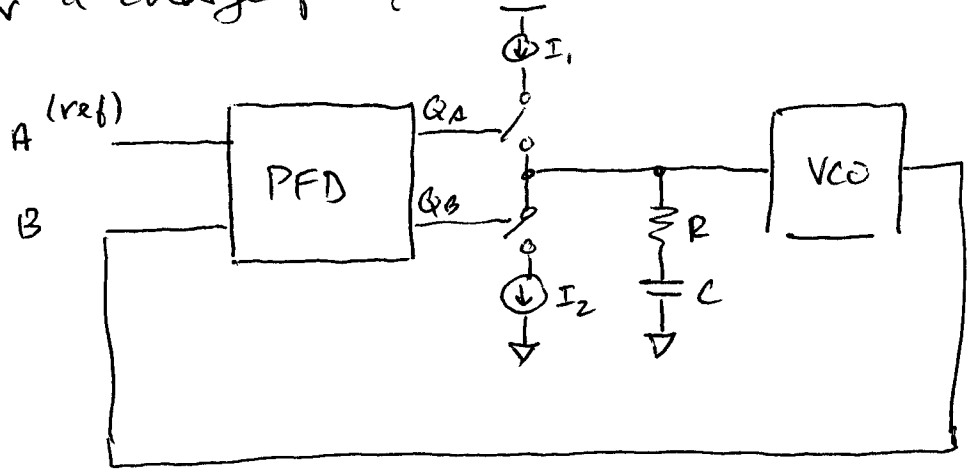
4. 0 phase offset

5. Not tolerant of input signal dropout.
   → ok for freq. synthesis
   not good for fm detection

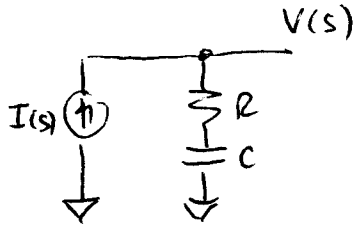
6. Output contains strong freq. component at f_r. Loop filter must be used to attenuate.

Charge Pump Loop Filter

The PFD output consists of up and down pulses. These can drive the differential op-amp based active filter shown previously, or a charge pump can be used.



DC gain is infinite since capacitor can charge up or down with charge = $I_1 T$ or $I_2 T$ for each pulse of width T.



$$\frac{V(s)}{I(s)} = F(s) = \frac{sRC+1}{s}$$

If both Q_A and Q_B reach full amplitude, the charge pump filter will assure zero phase difference between A and B, otherwise $V_{cont} \to \infty$

Lock and Capture Behavior

Up until now we have assumed that the loop is locked: $\phi_{out} = \phi_{in}$; $\omega_{out} = \omega_{in}$.

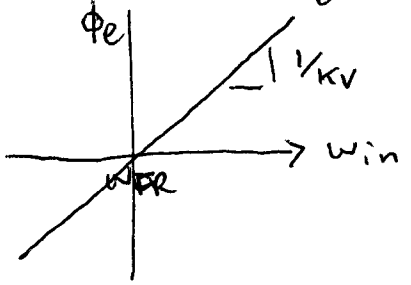
But, we have seen that some finite phase error is necessary to drive the VCO. This is kept small if K_V is large.

(1) Static Tracking Suppose we change the input frequency slowly so that the loop remains locked. How far can we change ω_i?

(2) Dynamic Tracking change input frequency as a step: $\Delta\omega$.

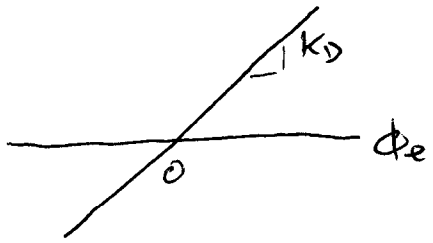
Must consider both cases.

(1) let ω_{in} vary from the ω_{FR} of the VCO.

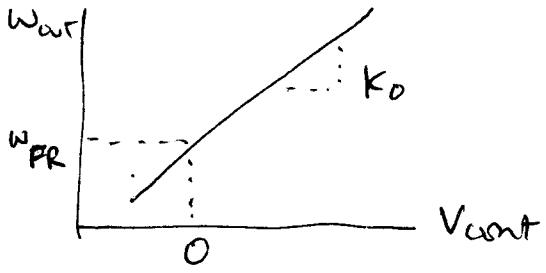


phase error must increase

This drives the PD output as well



and after filter, the control voltage drives the VCO frequency higher.



As long as those keep changing monotonically, the PLL will track.

Sooner or later, the PD or VCO will become non-monotonic or will saturate. Then lock will be lost.

So, the lock or tracking range is

$$\Delta\omega_L = \pm K_D K_O \cdot (\text{PD range}) = \pm K_V \frac{\pi}{2}$$

$\pi/2$ for XOR

— OR —

$\Delta\omega_L = \pm \frac{1}{2}$ VCO frequency range.

(2) frequency step, $\Delta\omega$

Large $\Delta\omega$: we calculated the steady state phase error for a freq. step $\phi_{ss} = \frac{\Delta\omega}{K_V}$ for TYPE 1

$= 0$ for TYPE 2

(if gain $\to \infty$ at $\omega =$

But, the loop responds with an exponential envelope $e^{-\sigma t} = e^{-\omega_n \zeta t}$, so the VCO will lose lock temporarily until the V_{cont} catches up.

If $\Delta\omega$ is as large as $\Delta\omega_L$, can the loop relock?

Acquisition or capture.

$$\left.\begin{aligned} \omega_{in} &= \omega_{FR} + \Delta\omega \\ \omega_{out} &= \omega_{FR} \end{aligned}\right\} \text{ loop out of lock}$$

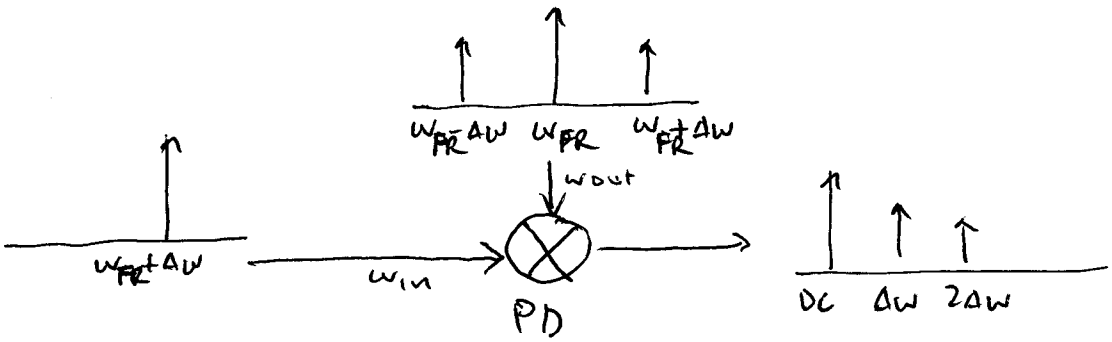
output of phase detector now has components at $\Delta\omega$ and $2\omega_{FR}+\Delta\omega$.
The loop filter removes the $2\omega_{FR}$ component

$\Delta\omega$ is applied to the VCO control voltage and will modulate (FM) the output frequency.

assume narrowband FM

$$V_{out}(t) = A\cos\omega_0 t - \frac{K_0}{\Delta\omega} A_m \sin(\omega_0 t)\sin(\Delta\omega t)$$

we have sidebands on output



PD is a mixer. We get a DC component that tries to relock the loop by driving VCO up.

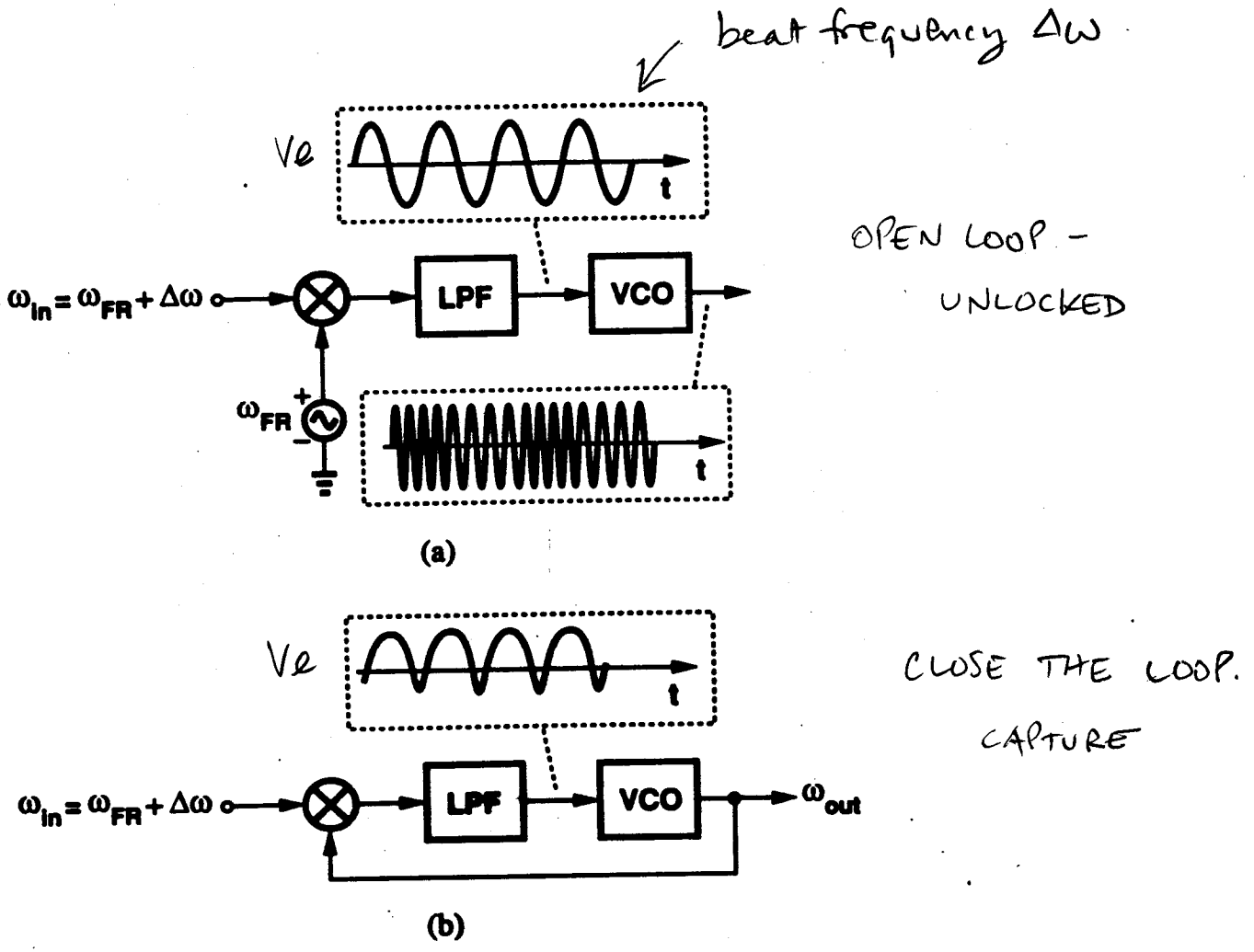


Fig. 22 Acquisition behavior in time domain.

Why is capture range less than lock range?

$\omega_{IN} \neq \omega_{FR}$ $\quad\quad$ $\Delta\omega = |\omega_{IN} - \omega_{FR}|$

Output of PD will have frequency component at $\Delta\omega$.

When filtered by the loop filter,

$$V_{cont} = V_{PD}(t) \underbrace{|F(\Delta\omega)|}_{\text{always} < 1}$$

Hence, if loop filter has a narrow BW, only small deviations from ω_{FR} can be captured without help from a frequency acquisition PD circuit.

Lock range is determined by the DC loop gain. Loop stays locked for small changes $\Delta\omega$.

Capture range is determined by the loop filter frequency response.

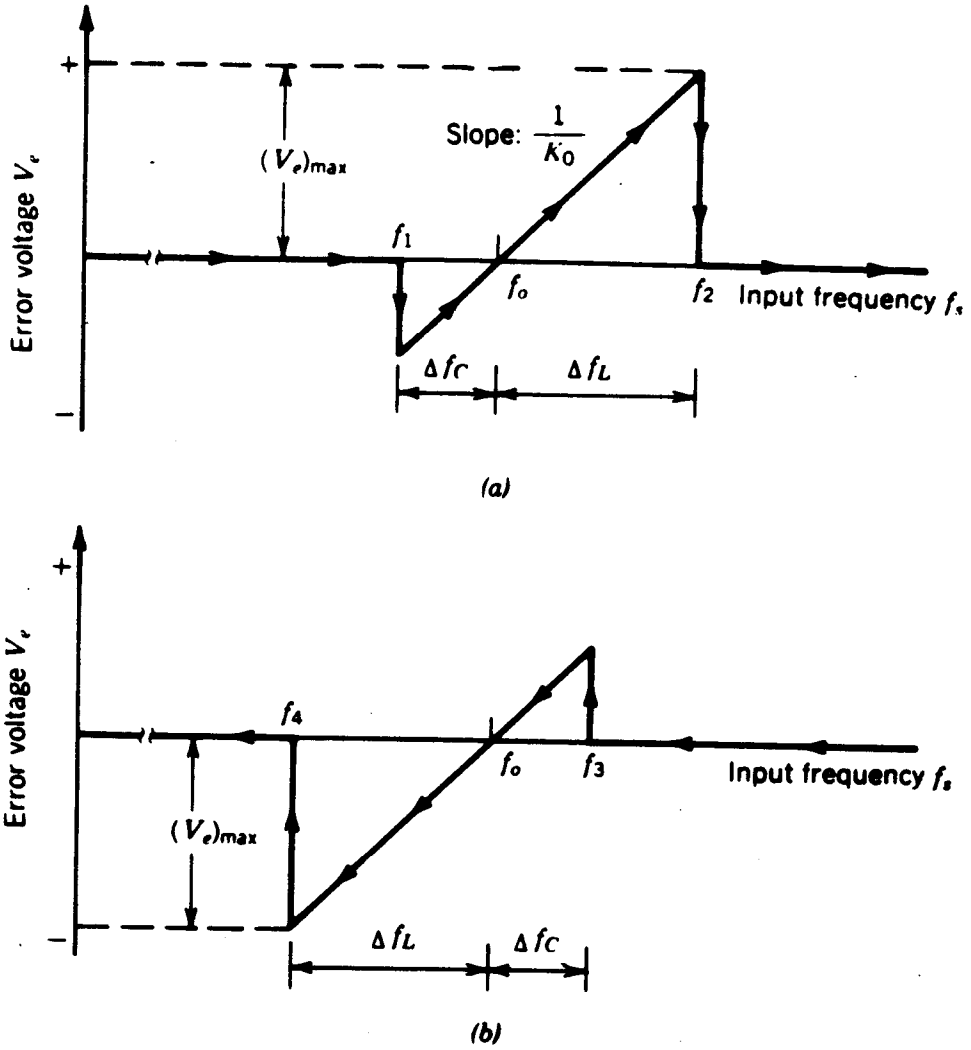


FIGURE 12.3. Typical PLL frequency-to-voltage transfer characteristics: (*a*) Slowly *increasing* input frequency; (*b*) *decreasing* input frequency.

What factors should be considered when choosing PLL bandwidth?

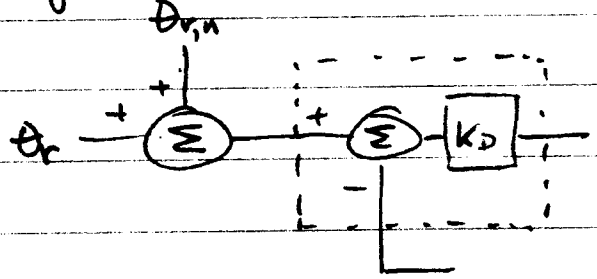
Lock-in time. Varies inversely with loop ω_{3dB}

Capture range may also be affected as discussed.

Noise. The loop filter and feedback shape the VCO phase noise spectrum.

For freq. synthesis, we are interested in low phase noise.

How is the reference phase noise influenced by the loop?



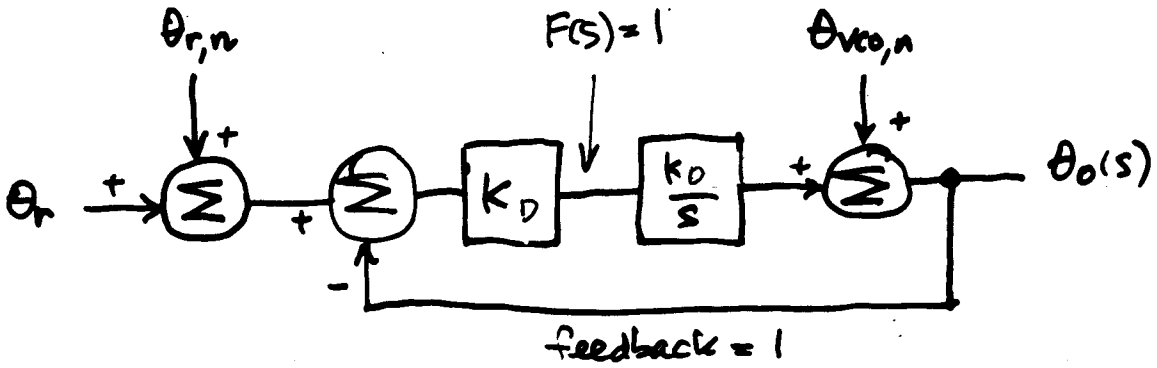
$$\frac{\theta_o}{\theta_{r,n}} = \frac{K_D K_o}{s + K_D K_o} = \frac{1}{1 + (1/K_D K_o)s} \to 0 \text{ as } s \to \infty$$

→ We see the loop acts as LPF for reference noise. Outside the loop BW, reference noise is attenuated

→ The loop filter, F(s), when present will also reduce ref. noise.

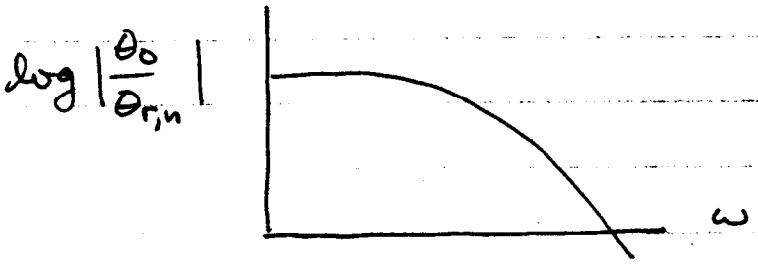
BUT: ref. noise can be small in freq. synthesizer

Phase Noise filtering in PLL :



$$\frac{\theta_o(s)}{\theta_{r,n}} = \frac{K_D K_o}{s + K_D K_o}$$ low pass

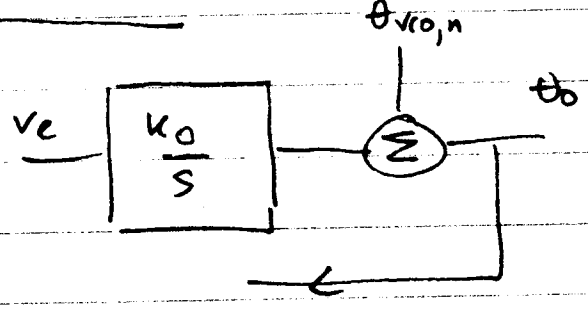
$$\frac{\theta_o(s)}{\theta_{vco,n}} = \frac{1}{1 + K_D K_o / s}$$ high pass



For second-order loop, we have even more noise shaping:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \begin{array}{l} \to 1 \text{ at } s = 0 \\ \to 0 \text{ as } s \to \infty \end{array}$$

what about VCO noise?



$$\frac{\theta_o}{\theta_{VCO,n}} = \frac{\text{fwd path gain}}{1 + T} = \frac{1}{1 + K_D K_O / s}$$

$$= \frac{1}{1 + 1/(+/K_D K_O)s} \to 1 \quad \text{as } s \to \infty$$

HIGH PASS

$\omega_{3dB} = K_D K_O$ also

Second order with simple LPF:

$$\frac{\theta_o(s)}{\theta_{VCO,n}} = \frac{s(s + \omega_{LPF})}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

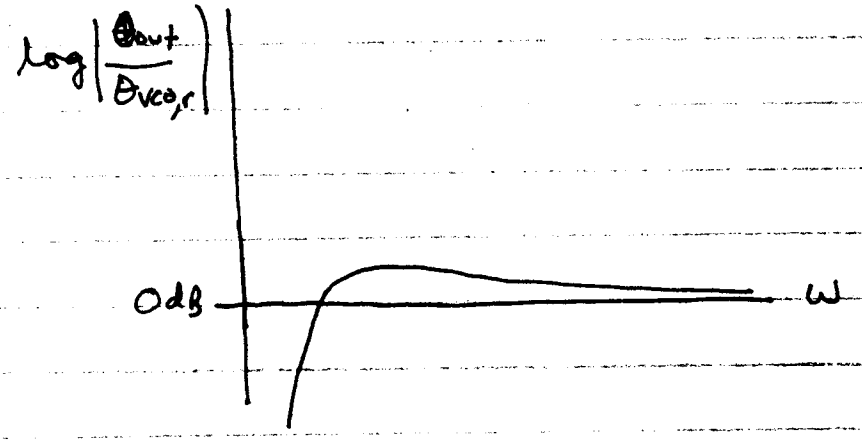
two zeros

$\omega_{z1} = 0$

$\omega_{z2} = -\omega_{LPF}$

Also high pass.

When $\theta_{vco,n}$ varies slowly (small s), the PD can correct for it using feedback. Once outside the loop bandwidth, the VCO noise is unaffected.



Thus, to get best VCO noise rejection loop bandwid should be maximized. This will also help the settling time needed for recovery from a step chan in ~~frequency~~ phase

$$\text{time constant} = \frac{1}{\zeta\omega_n}$$

$$\theta_o = \phi_1 \left[\cos\sqrt{1-\zeta^2}\,\omega_n t + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t\right] e^{-\zeta}$$

ϕ_1: phase step

This means that VCO noise is suppressed within loop BW but is transmitted <u>without attenuation</u> outside the bandwidth.

so: low BW is good for atten. ref. noise
(FM Detector appl.)

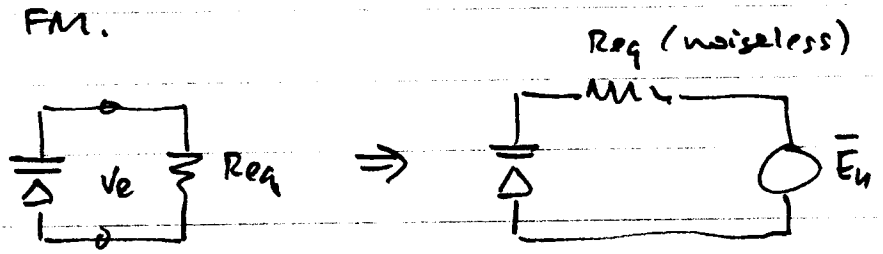
high BW is good for reducing VCO noise
(freq. synthesizer)

<u>What contributes to VCO phase noise?</u> (Leeson)

① P_s, Q_L, $\mathcal{L}(f) = \frac{P_{SSB}\ (1\ Hz\ BW)}{P_{carrier}} = \frac{kTF}{2P_s}\left(\frac{f_o}{2Q_L}\right)^2\left(\frac{1}{f_m}\right)$

② BUT: varactor tuning can also <u>add excess noise</u>

If K_{VCO} is high, thermal noise on V_c can generate FM.



$$\bar{E}_n = \sqrt{4kTR_{eq}B} \qquad \Delta f_{VCO} = K_{VCO}\,\bar{E}_n$$

Broad tuned VCOs can have 20-40 dB more noise than same osc. non-reactance tuned. VCOs.

③ Good shielding and filtering is essential to control excess noise and spurs.